EE 505

Lecture 24

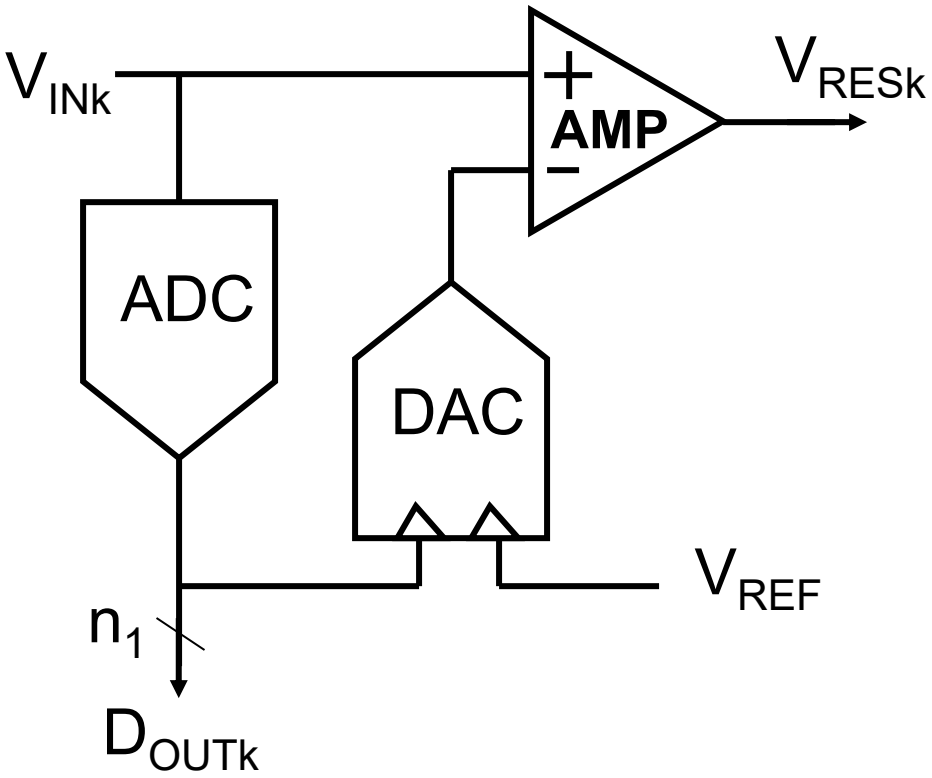
ADC Design

– Pipeline

Review from last lecture

Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

- Parameterization of Stage k
  - Amplifier
    - Closed-Loop Gain
      - From input – m1k
      - From DAC – m2k
      - From offset – m3k
    - Offset Voltage - V_{OSk}
  - DAC
    - V_{DACki}
  - ADC
    - Offset Voltages - V_{OSAki}
  - Out-Range Circuit (if used and not included in ADC/DAC)
    - DAC Levels - V_{DACBki}
    - Amplifier Gain – m4k



Review from last lecture

Solution of the 2n Linear Equations

$$V_{in} = \underbrace{\left\{ d_1\left[\left(\frac{m_{21}}{m_{11}}\right)V_{DAC1}\right] + d_2\left[\left(\frac{m_{22}}{m_{11}m_{12}}\right)V_{DAC2}\right] + \ldots + d_n\left[\left(\frac{m_{2n}}{m_{11}m_{12}\ldots m_{1n}}\right)V_{DACn}\right] + \frac{V_{REF}}{2^{n+1}} \right\}}_{\text{Term involving digital output codes}}$$

$$+ \underbrace{\left\{ \frac{m_{31}}{m_{11}}V_{OS1} + \frac{m_{32}}{m_{11}m_{12}}V_{OS2} + \ldots + \left(\frac{m_{3n}}{m_{11}m_{12}\ldots m_{1n}}\right)V_{OSn} \right\}}_{\text{Code-independent offset term}}$$

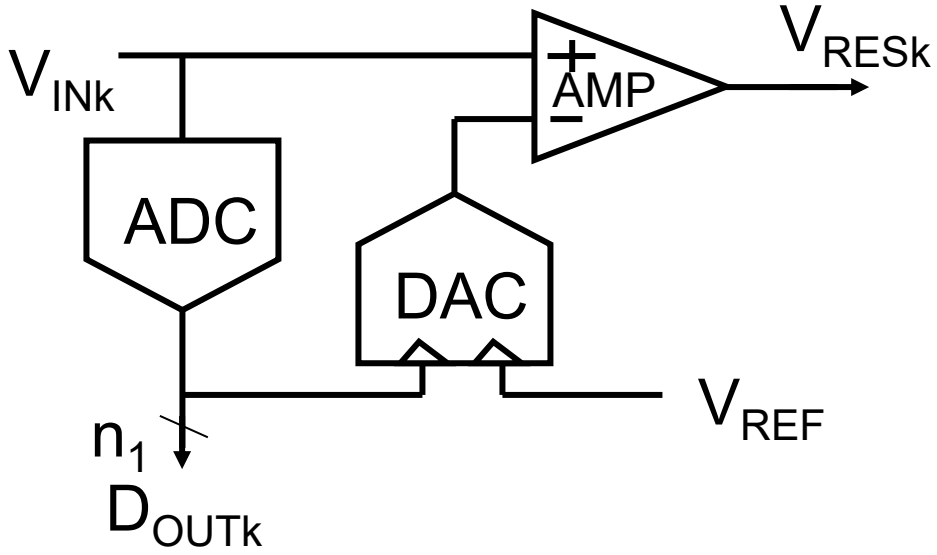
$$+ \underbrace{\left\{ \frac{V_{RESn}}{m_{11}m_{12}\ldots m_{1n}} - \frac{V_{REF}}{2^{n+1}} \right\}}_{\text{Code-dependent but can be bounded by ½ LSB with out-range strategy}}$$

Note: Will not even include last residue amplifier nor create V_{RESn}

Note: ADC errors do not affect linearity performance of pipelined structure but DAC outputs and weights are critical

Review from last lecture

Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

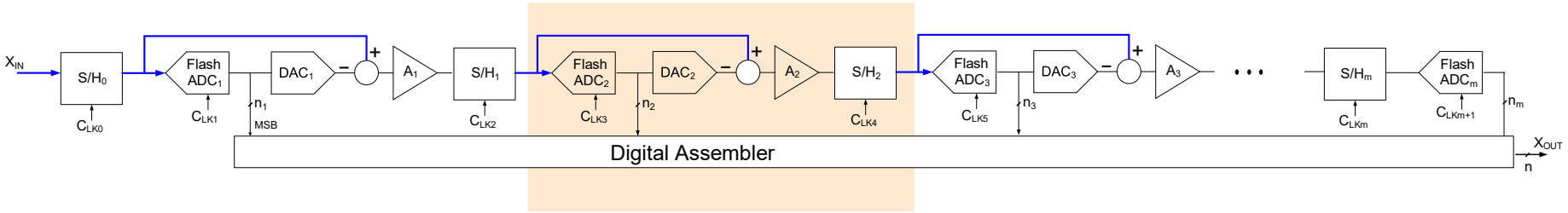


If more than 1 bit/stage is used and DAC is binarily-weighted structure

$$V_{RESk} = m_{1k} V_{ink} + m_{2k} \left(\sum_{j=1}^{2^{n_k}-1} d_{kj} V_{DACkj} \right) + m_{3k} V_{OSk}$$

Review from last lecture

Pipelined ADC



Claim: If the Amplifiers are linear, settling is complete, and over-range protection is provided, the pipelined ADC makes no nonlinearity errors if the output of the DACs are correctly interpreted

Implication: Flash ADC errors, offsets in comparators and amplifiers, and gain errors in amplifier and S/H do not degrade linearity performance of a well-designed pipelined ADC structure !!

Review from last lecture

Observations

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

form of α_k : $V_{DACk} \dfrac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$

- Substantial errors are introduced if α_k are not correctly interpreted!
- Some calibration and design strategies focus on accurately setting gains and DAC levels
- Analog calibration can be accomplished with either DAC level or gain calibration
- Digital calibration based upon coefficient identification does not require accurate gains or precise DAC levels

Review from last lecture

Observations (cont)

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

form of α_k : $V_{DACk} \dfrac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$

- If nonlinearities are avoided, data conversion process with a pipelined architecture is extremely accurate
- Major challenge at low frequencies is accurately interpreting the digital output codes

Review from last lecture

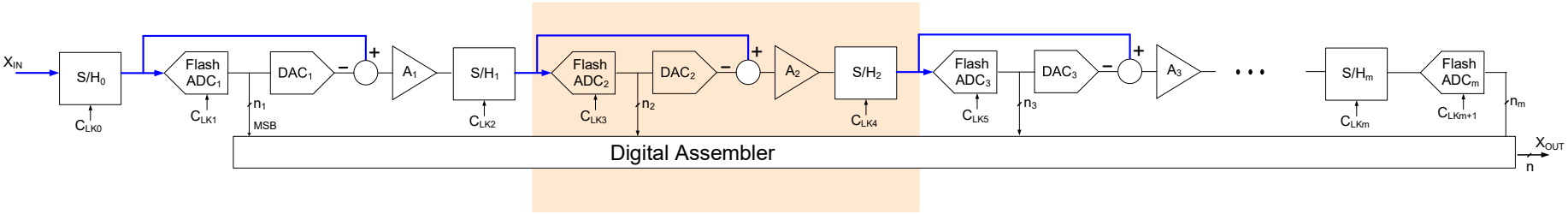
Observations (cont)

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

form of α_k : $V_{DACk} \dfrac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$

- If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable !

Intuitive View of Why Sub-ADCs do Not Cause Nonlinearity Errors



Claim: If the Amplifiers are linear, settling is complete, and over-range protection is provided, the pipelined ADC makes no nonlinearity errors if the output of the DACs are correctly interpreted

for 1 bit/stage

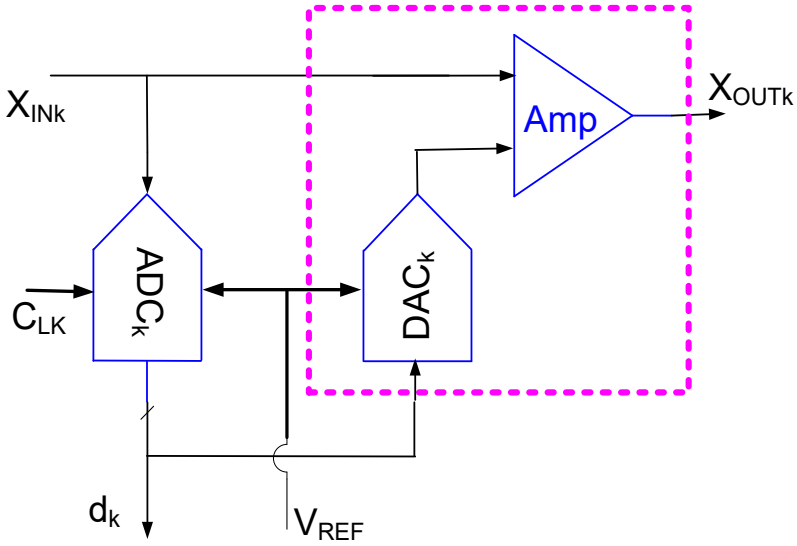
$$V_{in} = \left\{ d_1 \left[\left(\frac{m_{21}}{m_{11}} \right) V_{REF} \right] + d_2 \left[\left(\frac{m_{22}}{m_{11} m_{12}} \right) V_{REF} \right] + \ldots + d_n \left[\left(\frac{m_{2n}}{m_{11} m_{12} \ldots m_{1n}} \right) V_{REF} \right] + \frac{V_{REF}}{2^{n+1}} \right\} + V_{OSEQ} + \varepsilon$$

- ADCs determine whether a quantity is or is not subtracted from V_{REF} at each stage but the DAC determines how much is subtracted
- Keep subtracting smaller-and-smaller quantities from V_{IN} until residue is approx. 0 at end of last stage (and error caused by last sub-ADC will be small)
- If we know how much is subtracted from V_{IN} until residue vanishes, we know V_{IN}
- Over-range protection recovers errors caused by subtracting too much or too little

Performance Limitations of Pipelined ADCs

(consider amplifier, ADC and DAC issues)

- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
  - Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Inadequate open loop gain
    - Component mismatch
  - Power Dissipation
  - kT/C switching noise



Performance Limitations of Pipelined ADCs

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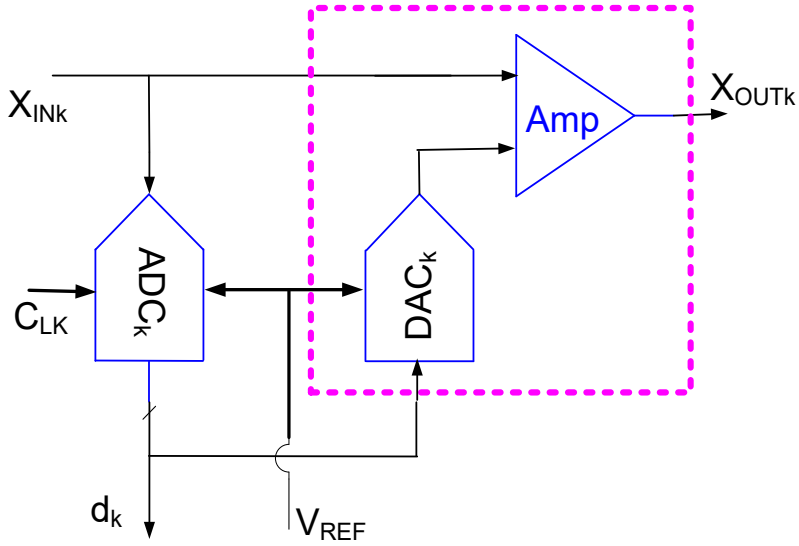


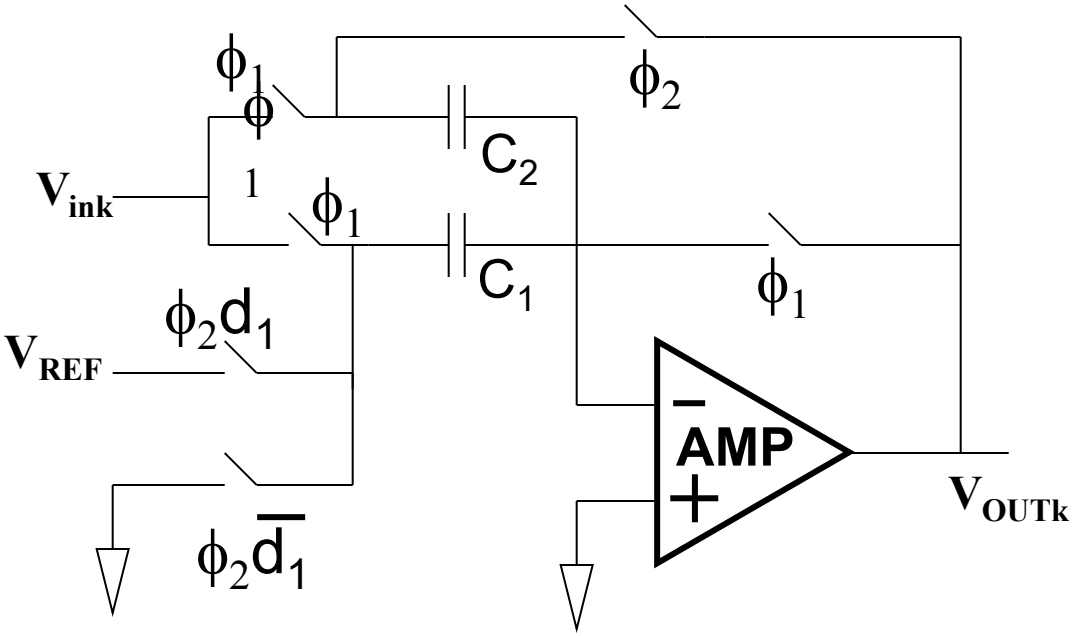
Pipelined Data Converter Design Guidelines

	Issue	Strategy
1.	ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	

Review – preparing for calibration :

Interstage Amplifiers

Typical Finite-Gain Inter-stage Amplifier
(shown single-ended with 1-bit/stage)



Ideally

$$V_{OUT} = V_{IN}\left(1+\frac{C_1}{C_2}\right) - d_1\left(\frac{C_1}{C_2}\right)V_{REF}$$

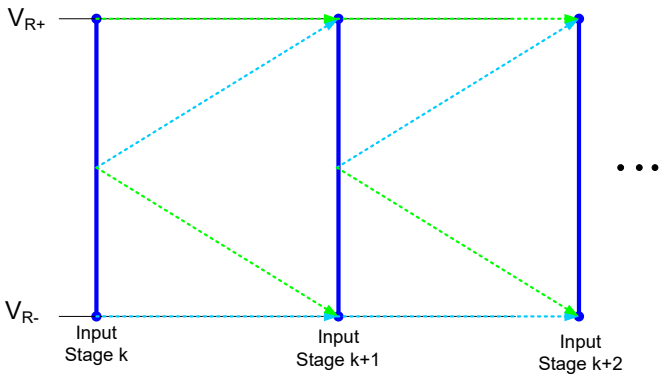
$$V_{OUT} = 2V_{IN} - d_1 V_{REF}$$

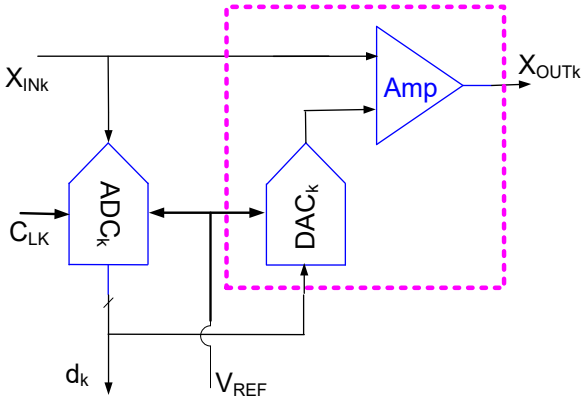
Gain =2.00000

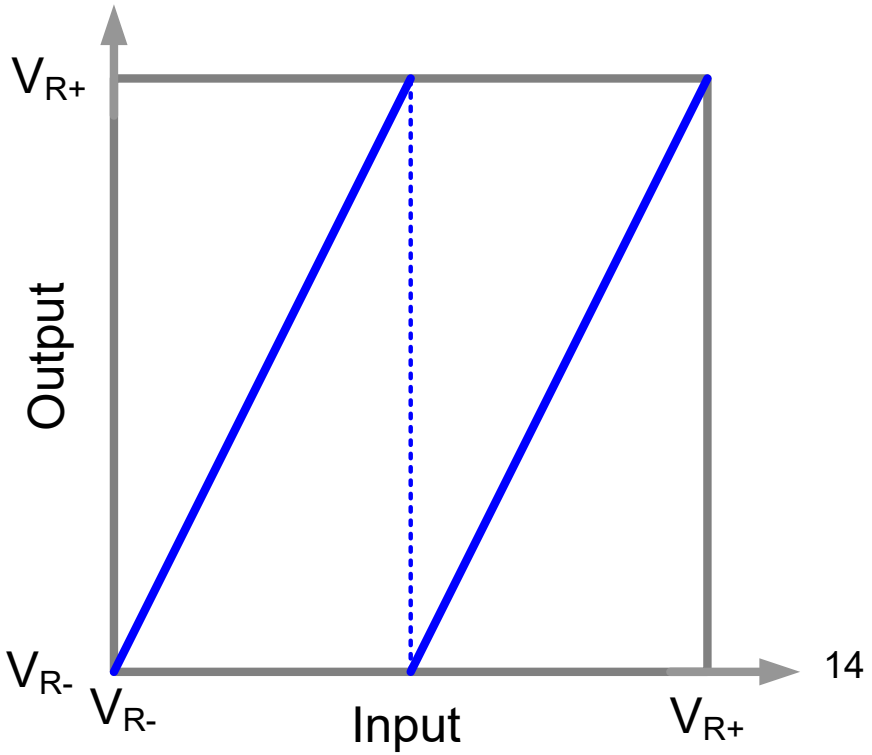
Review – preparing for calibration :

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

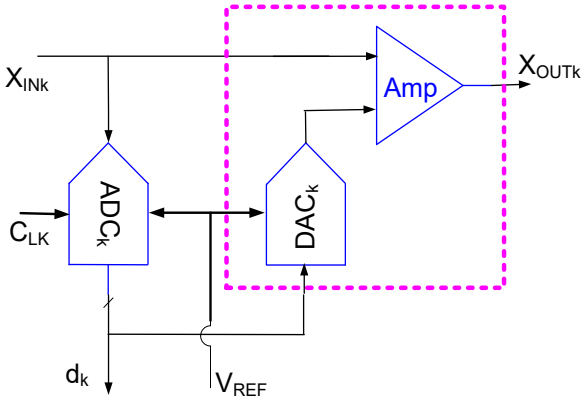




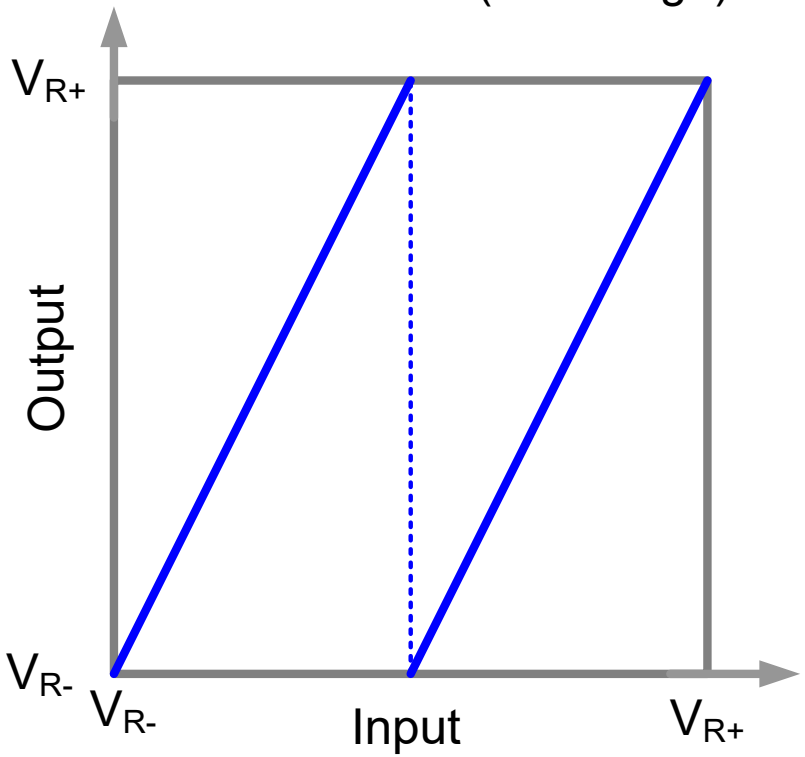


Review – preparing for calibration :

Interstage Amplifiers



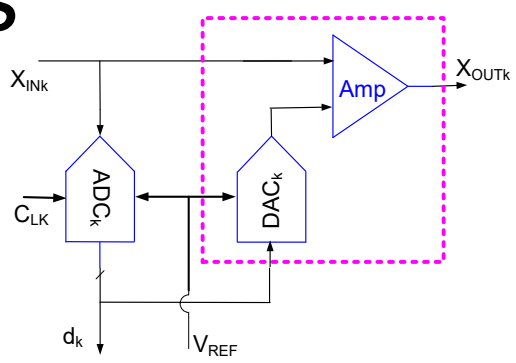
Ideal transfer characteristics (1 bit/stage)



But what really happens?

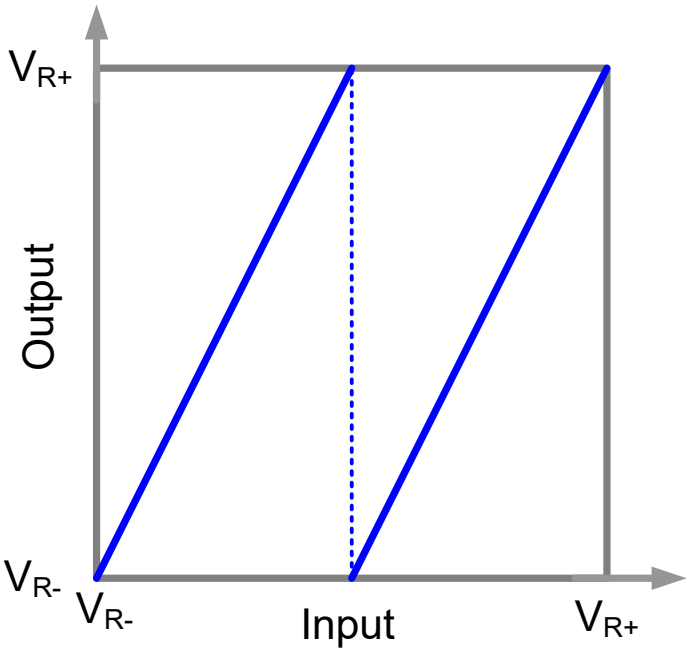
Review – preparing for calibration :

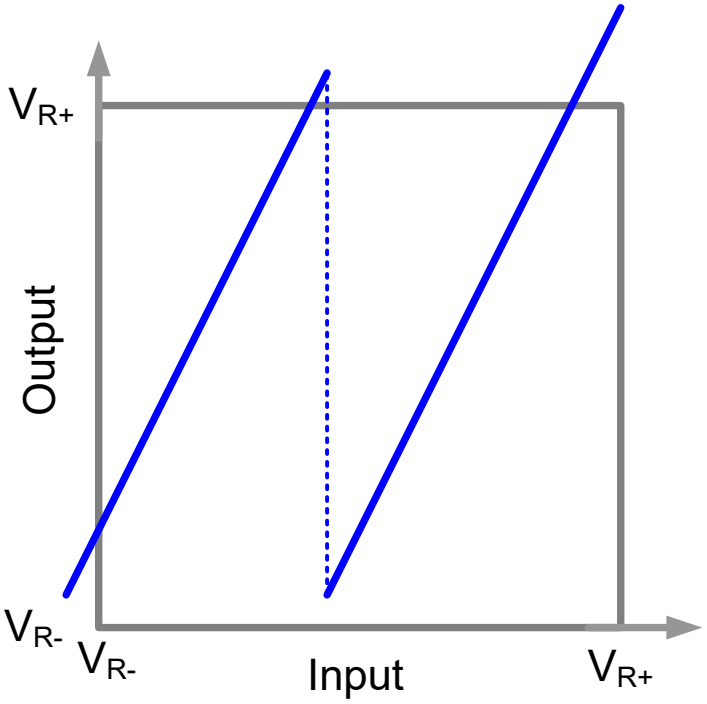
Interstage Amplifiers



Ideal transfer characteristics (1 bit/stage)

What are the effects of these errors?

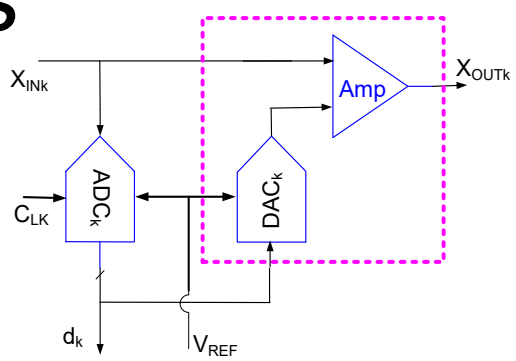




Effects of Simultaneous Errors

Review – preparing for calibration :

Interstage Amplifiers



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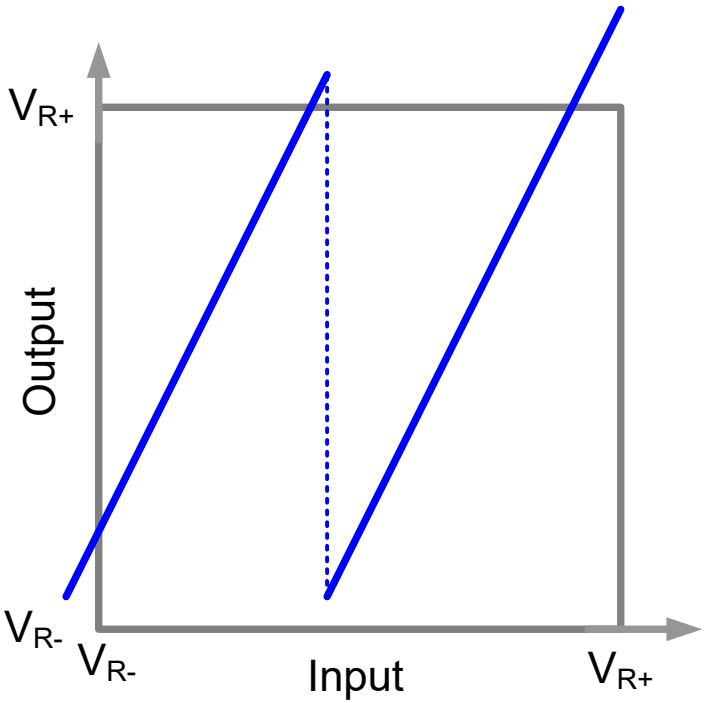
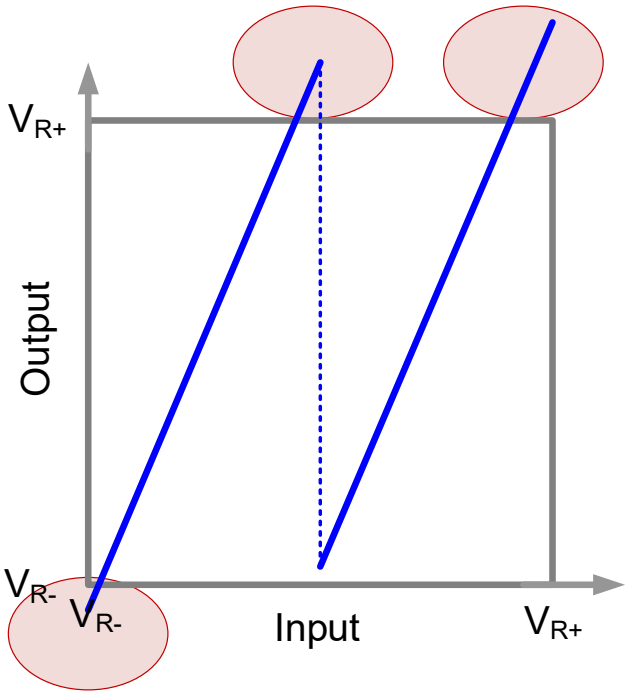
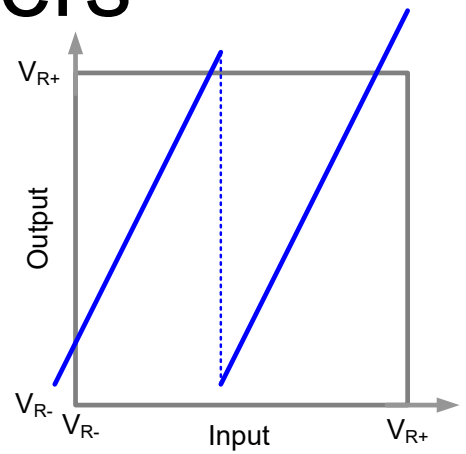




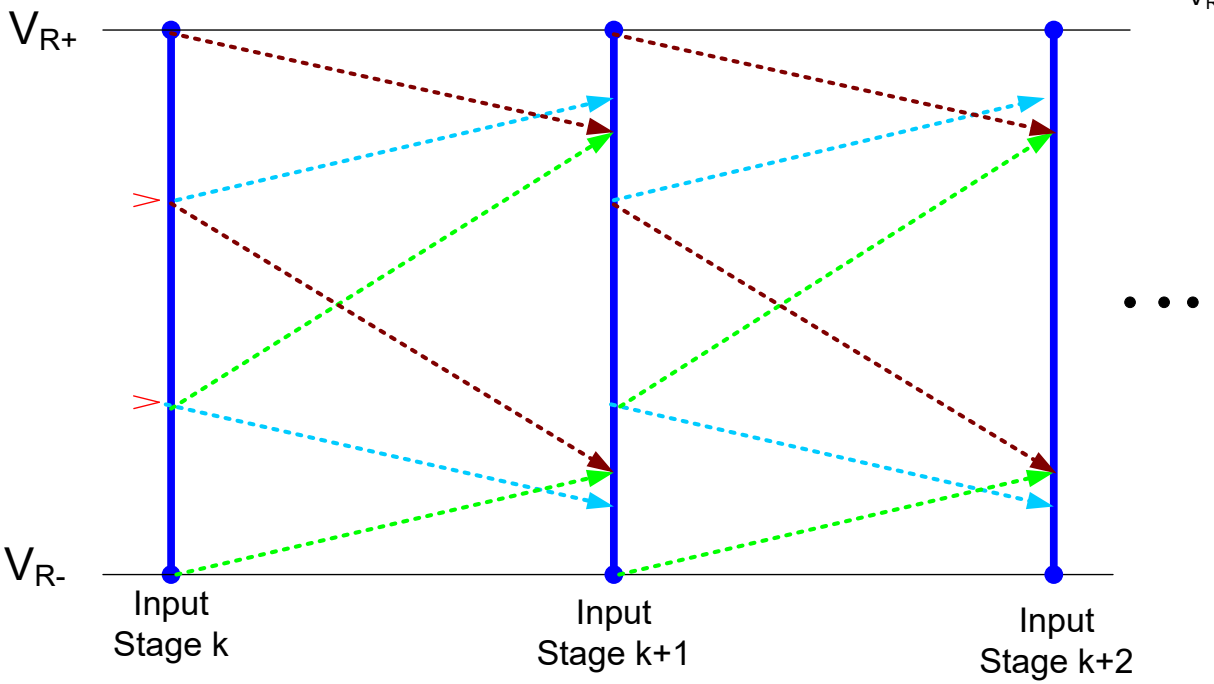
Review – preparing for calibration :

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



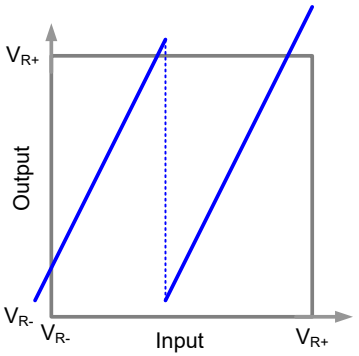
Over-range Protection



Extra comparator levels in ADC

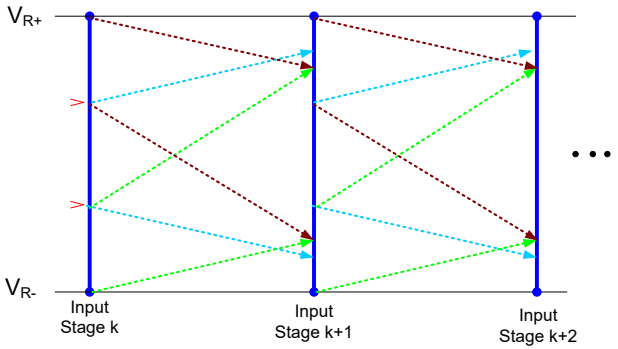
Review – preparing for calibration :

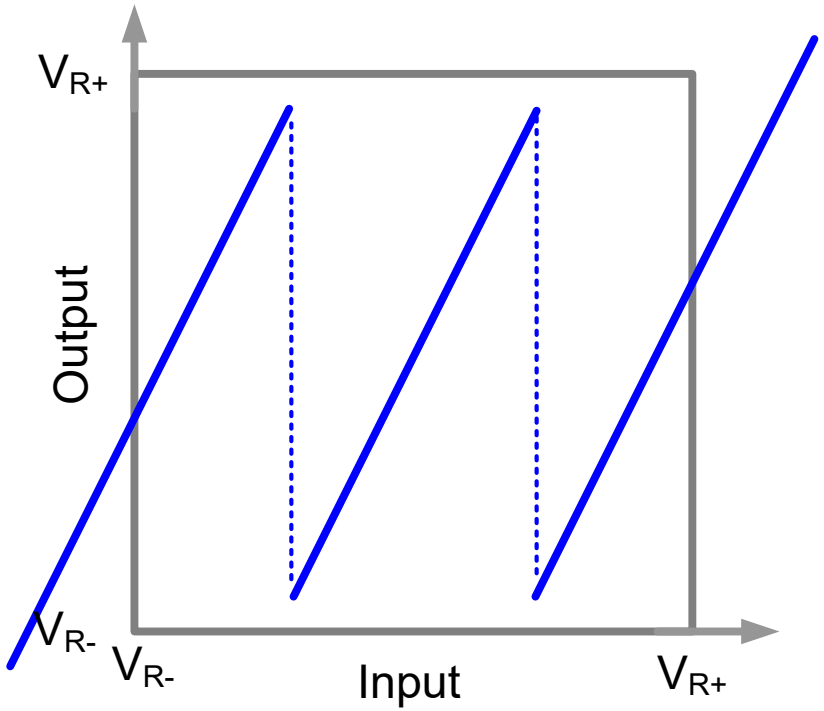
Interstage Amplifiers



Ideal transfer characteristics (1 bit/stage)

Over-range Protection

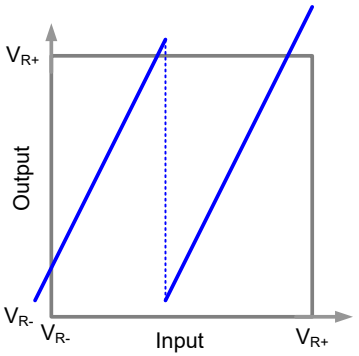




Extra comparator levels in ADC (1 extra comparator)

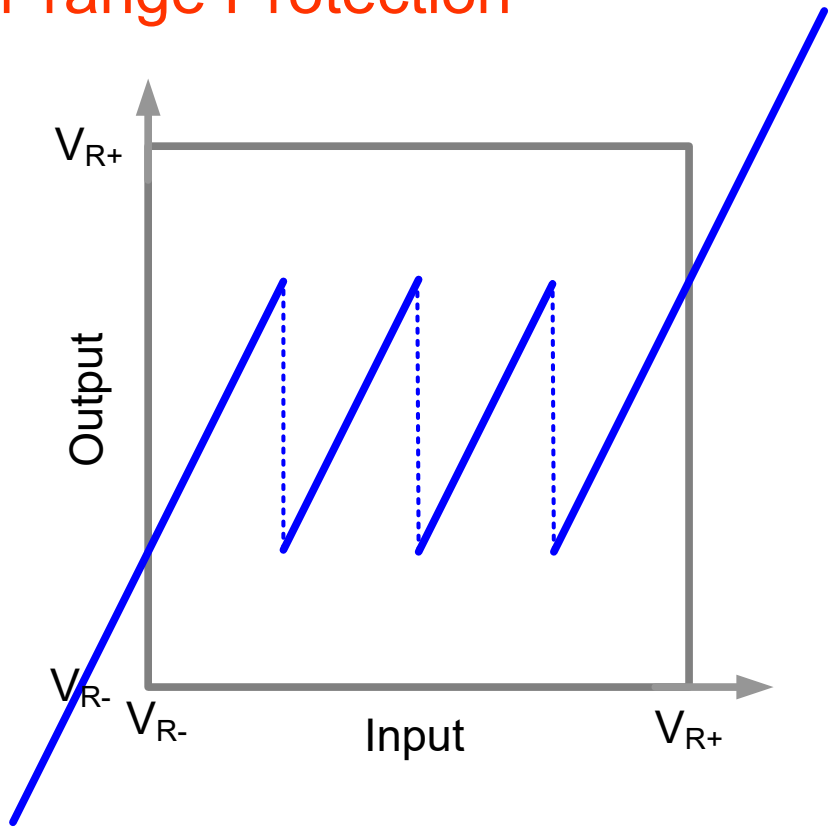
Review – preparing for calibration :

Interstage Amplifiers



Ideal transfer characteristics (1 bit/stage)

Over-range Protection

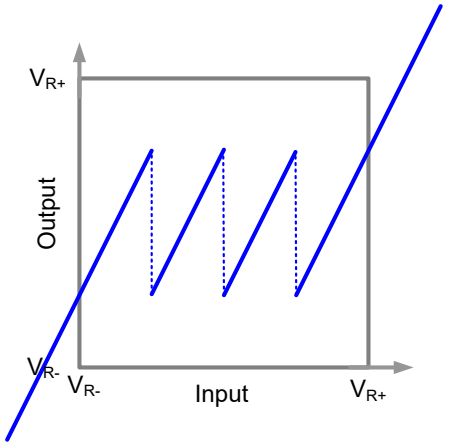


Extra comparator levels in ADC (2 extra comparators)

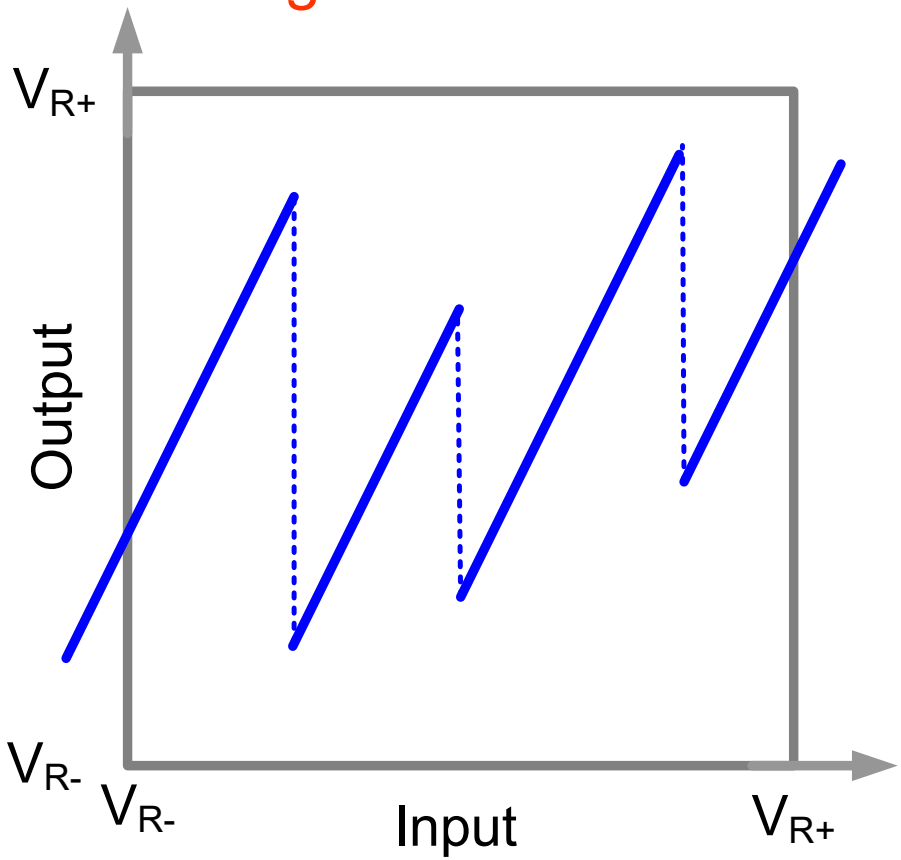
Review – preparing for calibration :

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



Over-range Protection



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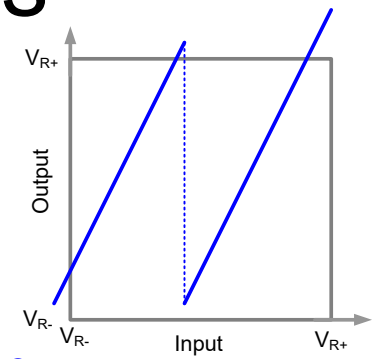
Review – preparing for calibration :

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



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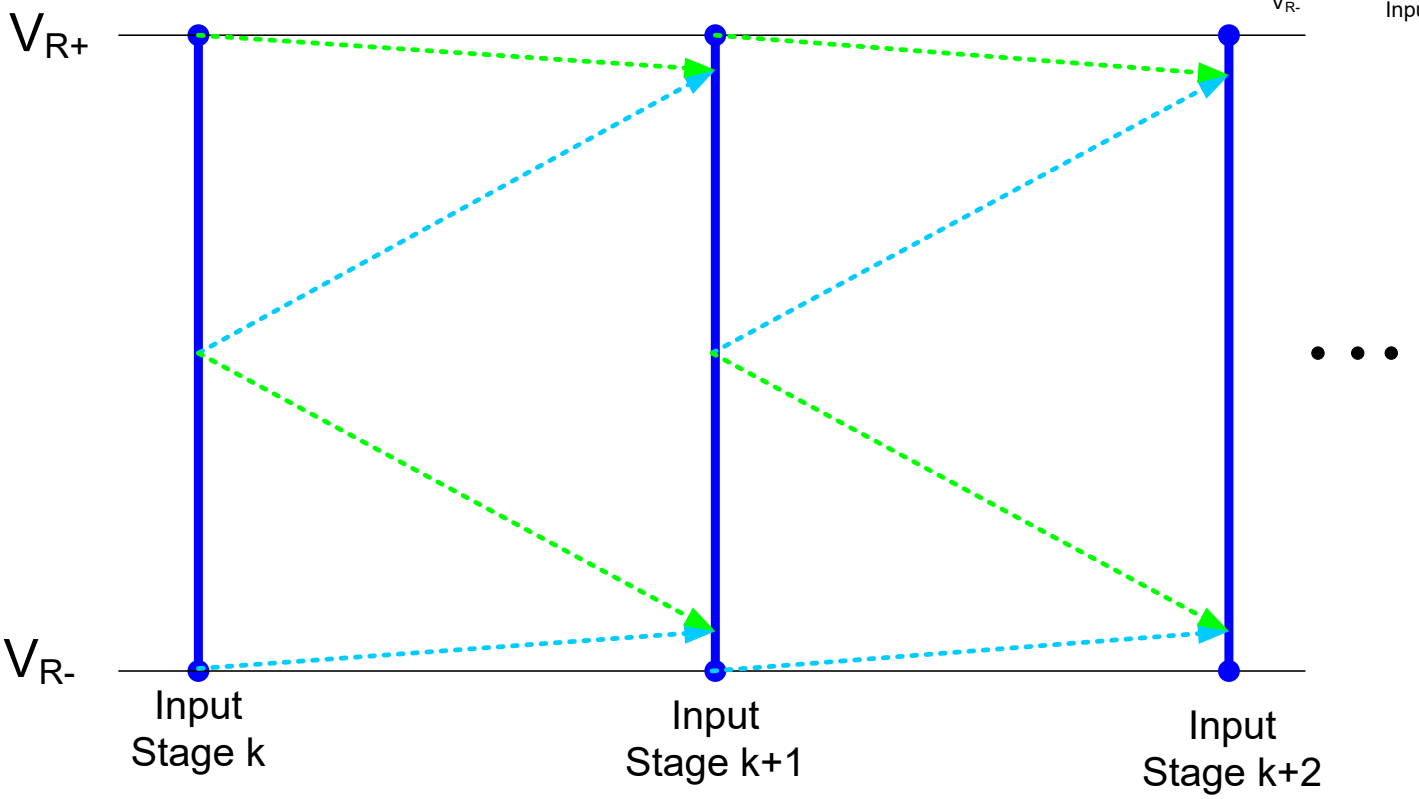

Sub-radix Structure

Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures

Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Correct interpretation of α_k's is critical	2. a) Accurately set α_k values b) Use analog or digital calibration

Performance Limitations of Pipelined ADCs

(consider amplifier, ADC and DAC issues)

- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
  - Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
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    - Component mismatch
  - Power Dissipation
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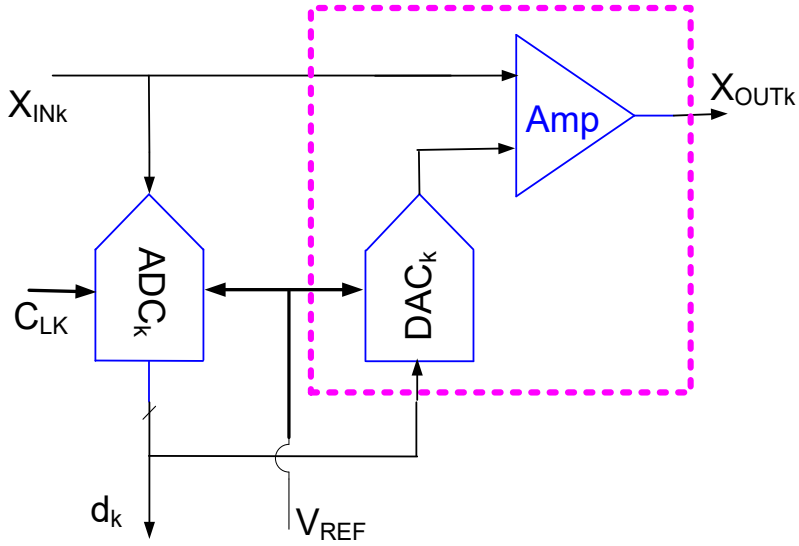
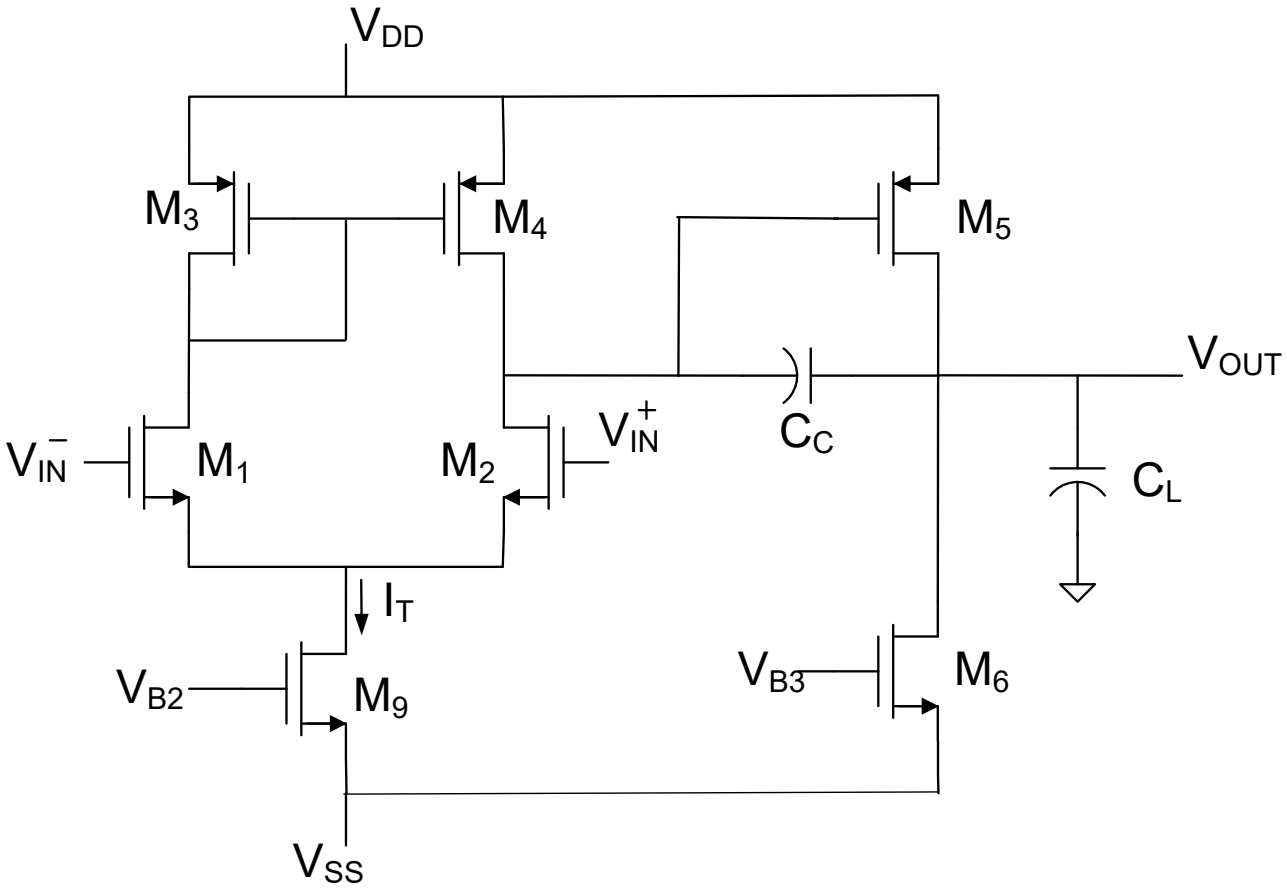


Amplifier Types used In Pipelined ADCs

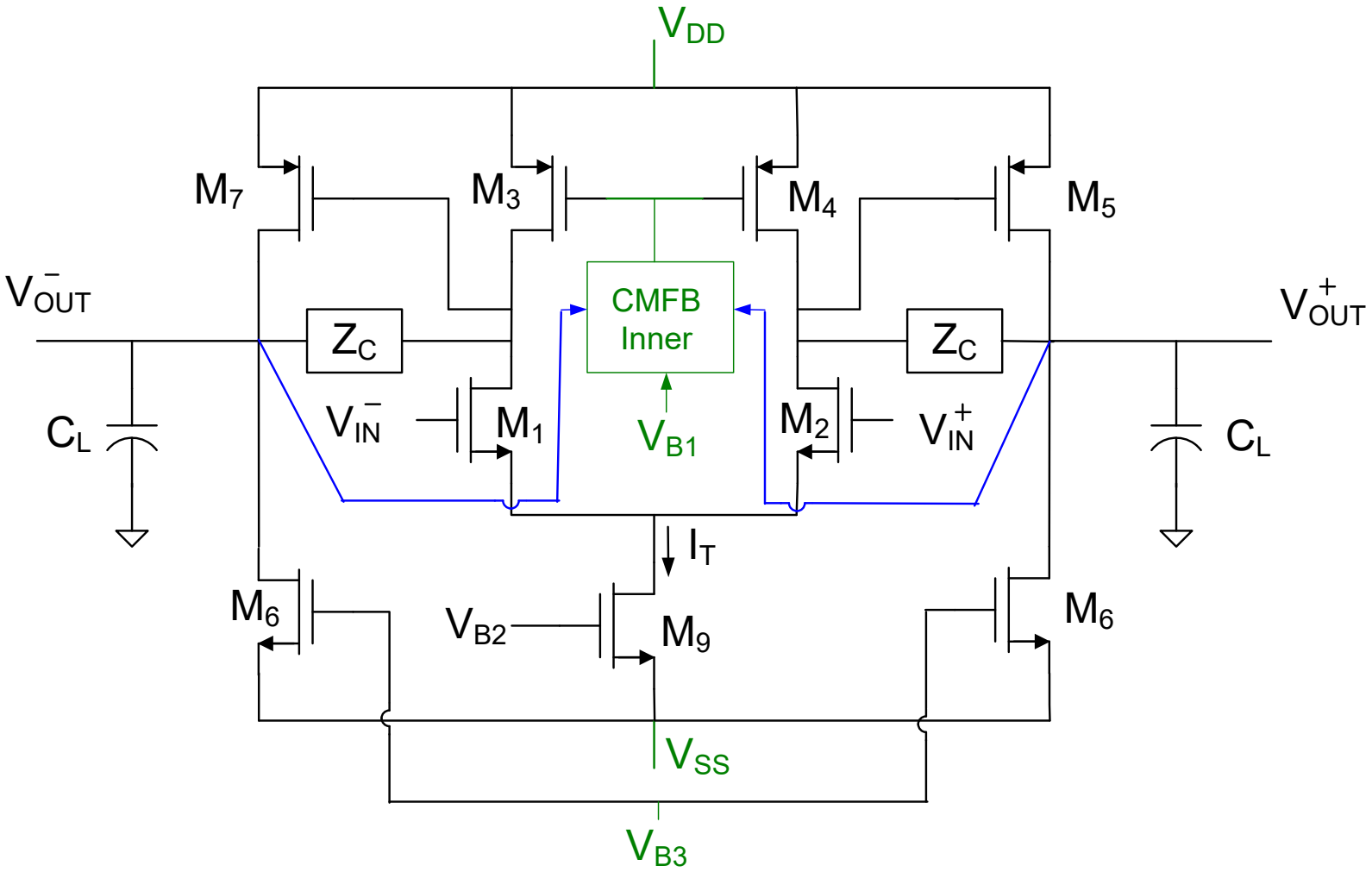
- Two-stage
- Cascode
  - Telescopic
  - Folded
- Regulated Cascode (Gain-boosted Cascode)
  - Telescopic
  - Folded
- Regenerative Feedback Gain Enhancement
- Two-Stage Cascode

Two-Stage



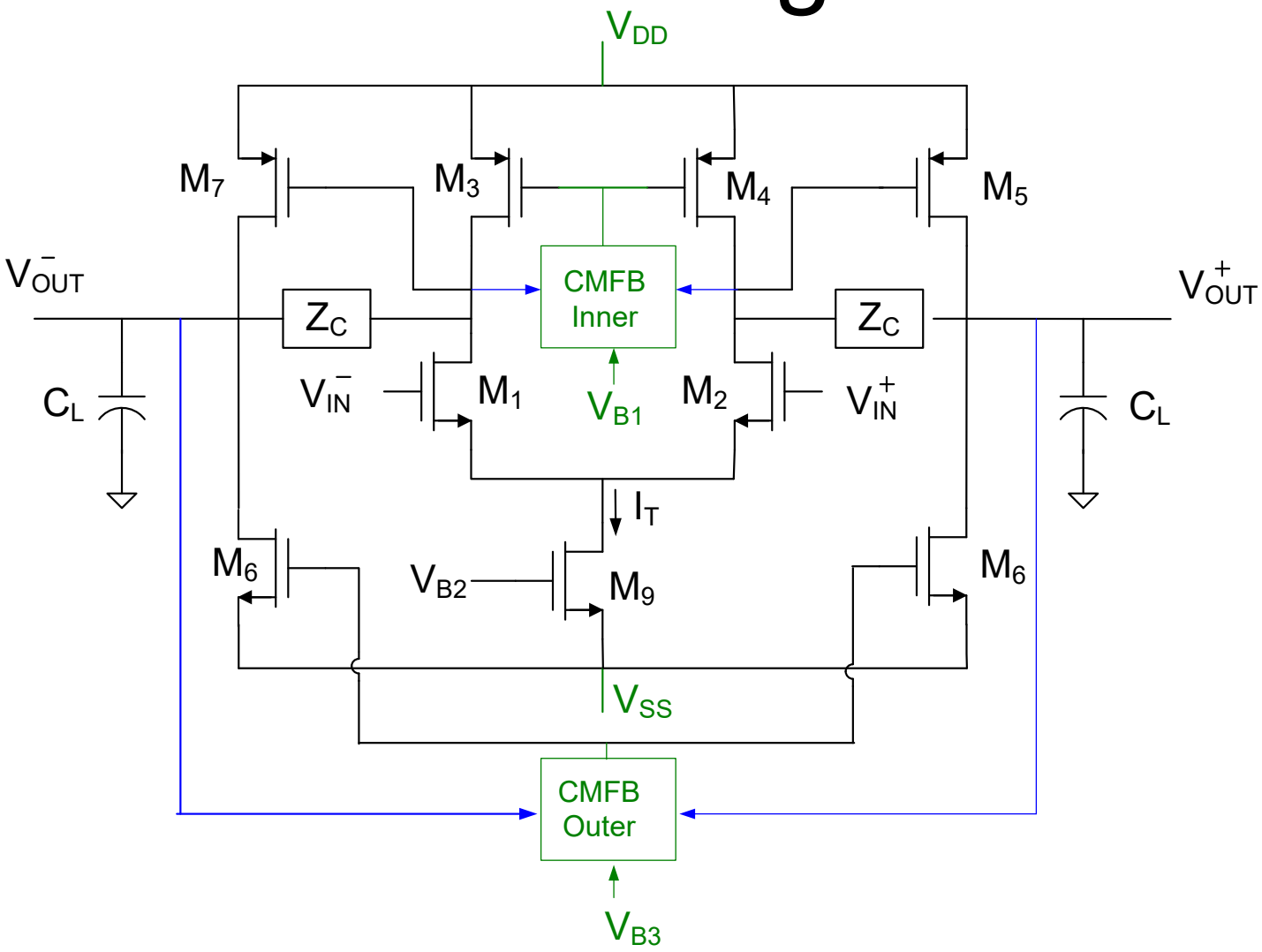
Single-Ended Output

Two-Stage



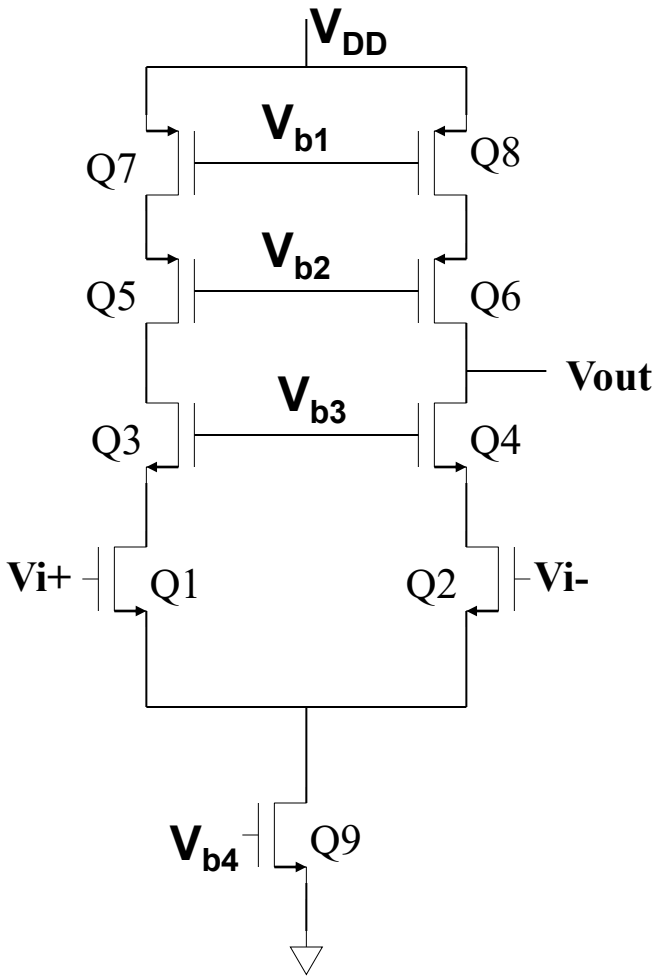
Fully Differential

Two-Stage



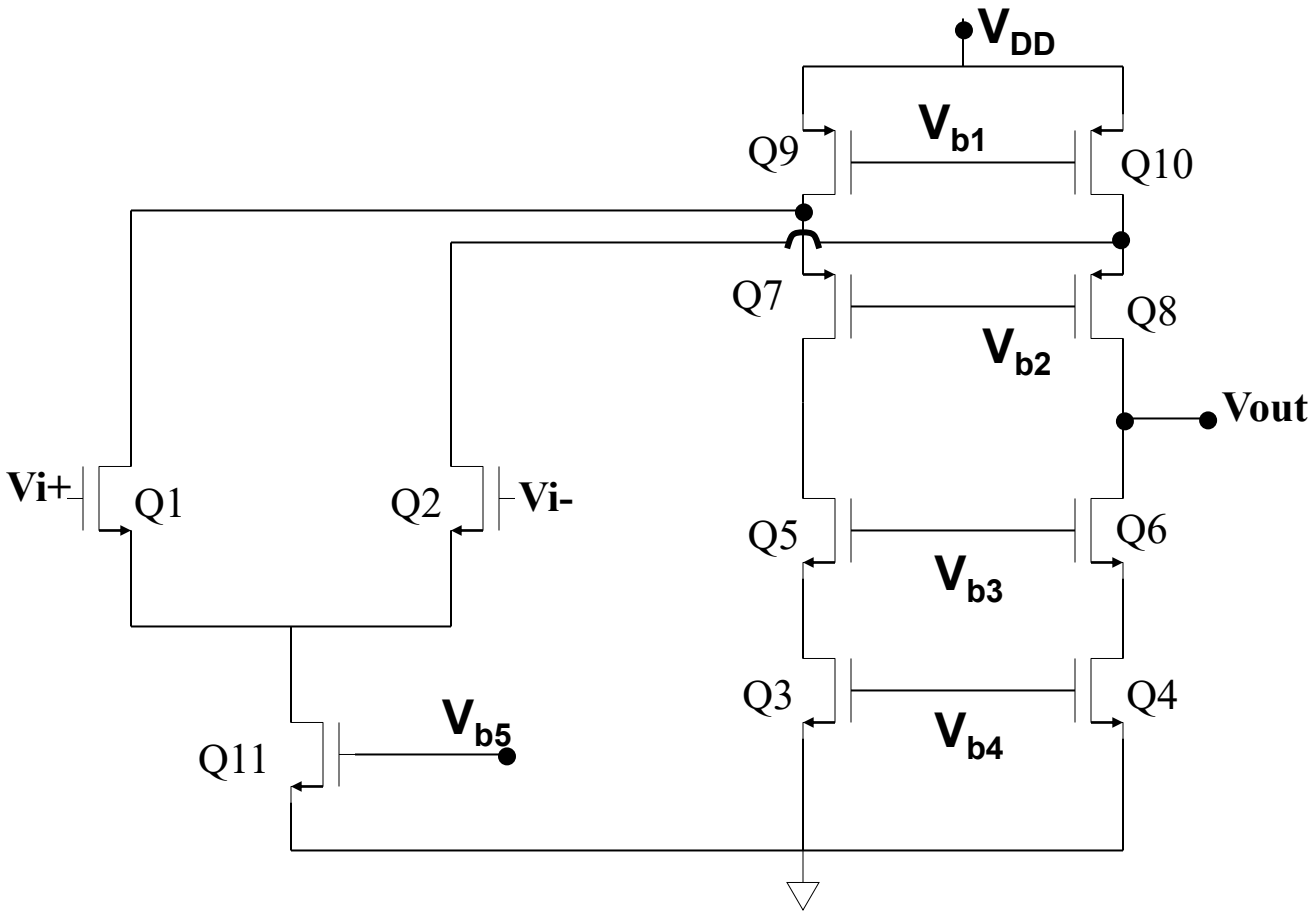
Fully Differential

Telescopic Cascode



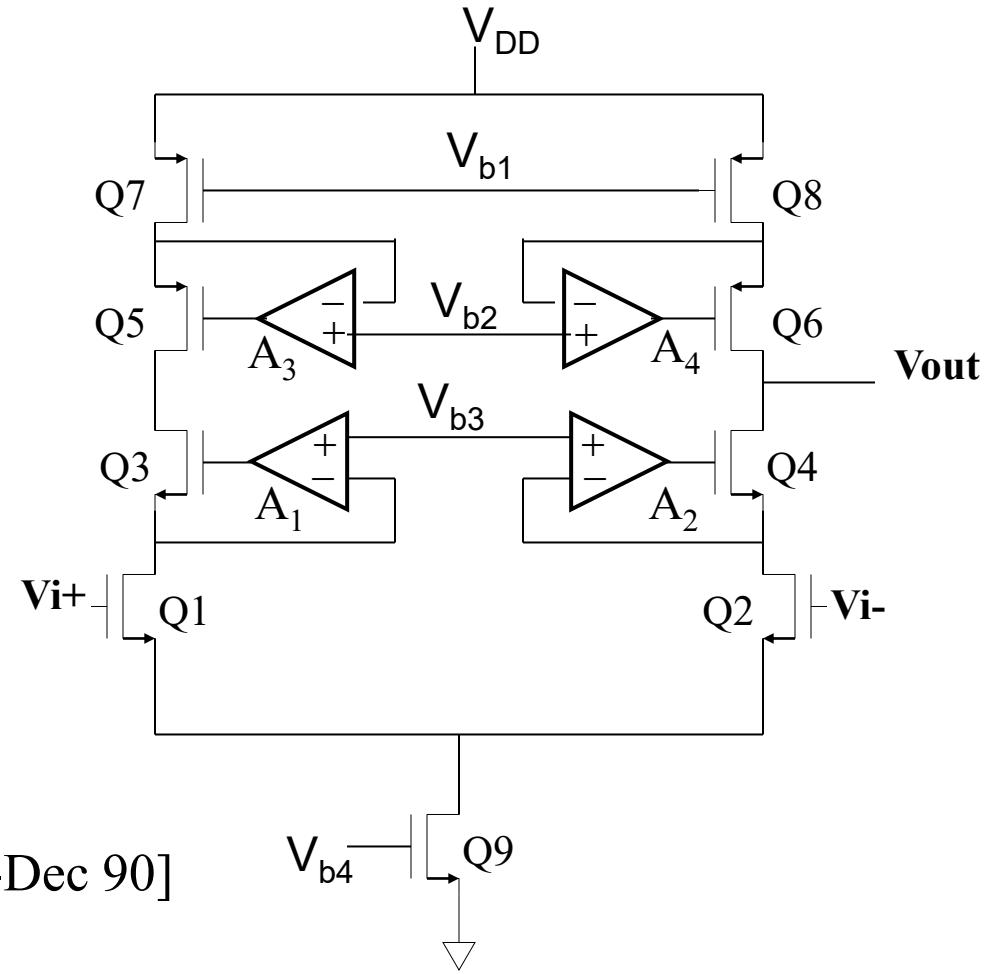
CMFB Not Shown

Folded Cascode Amplifier



CMFB Not Shown

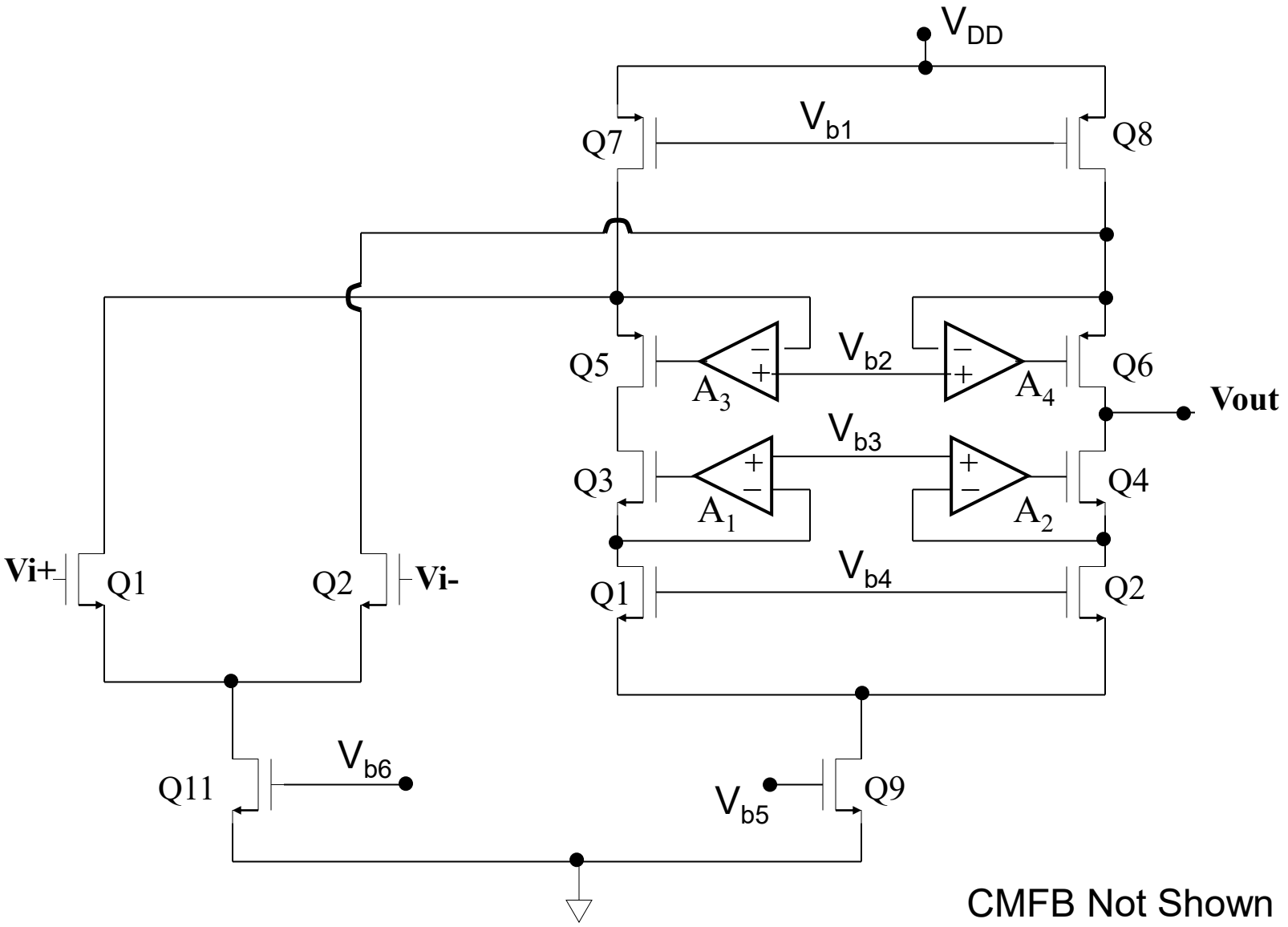
Gain-Boosted Telescopic Cascode



[Bult – JSSC-Dec 90]

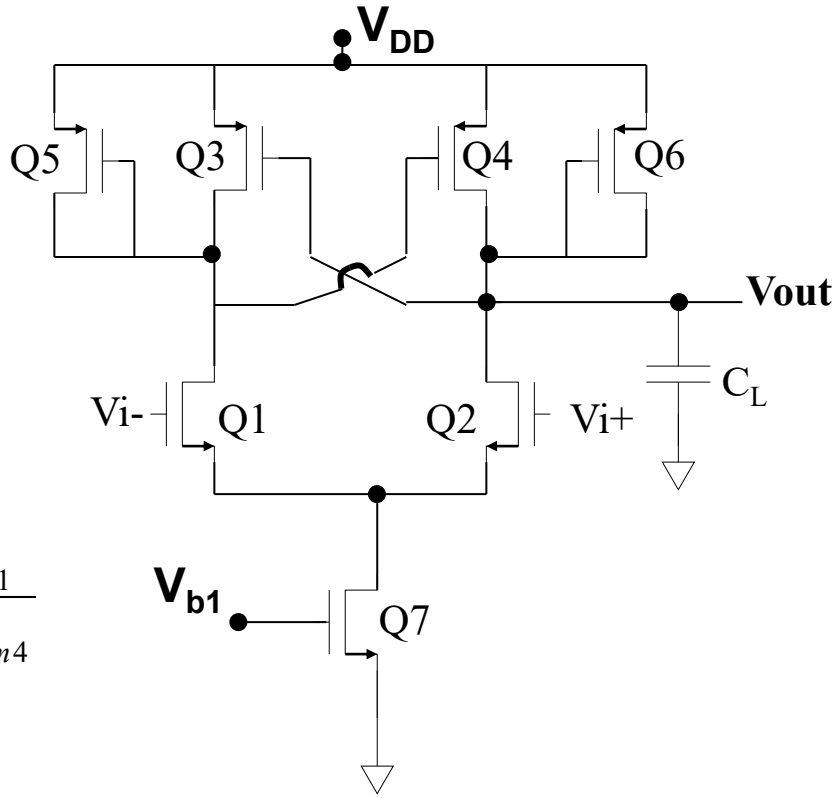
CMFB Not Shown

Gain-Boosted Folded Cascode



CMFB Not Shown

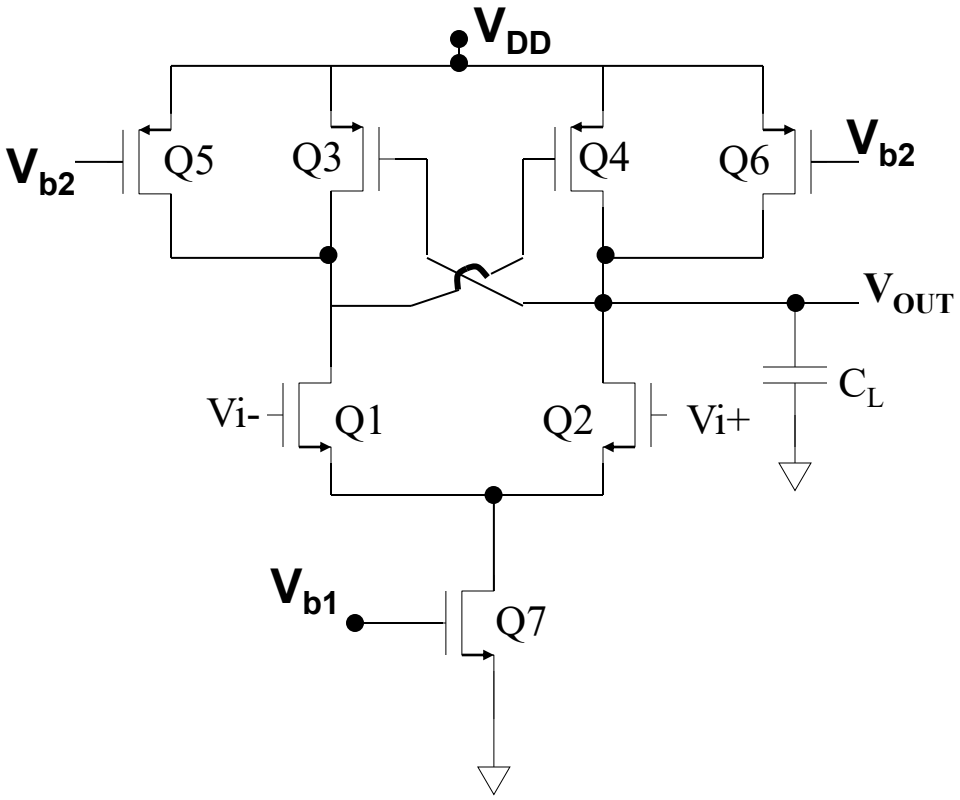
$-g_m$ Compensation Implementation



$$A_{VO} = \frac{(1/2)g_{ml}}{g_{o2} + g_{o4} + g_{06} + g_{m6} - g_{m4}} \approx \frac{(1/2)g_{ml}}{g_{m6} - g_{m4}}$$

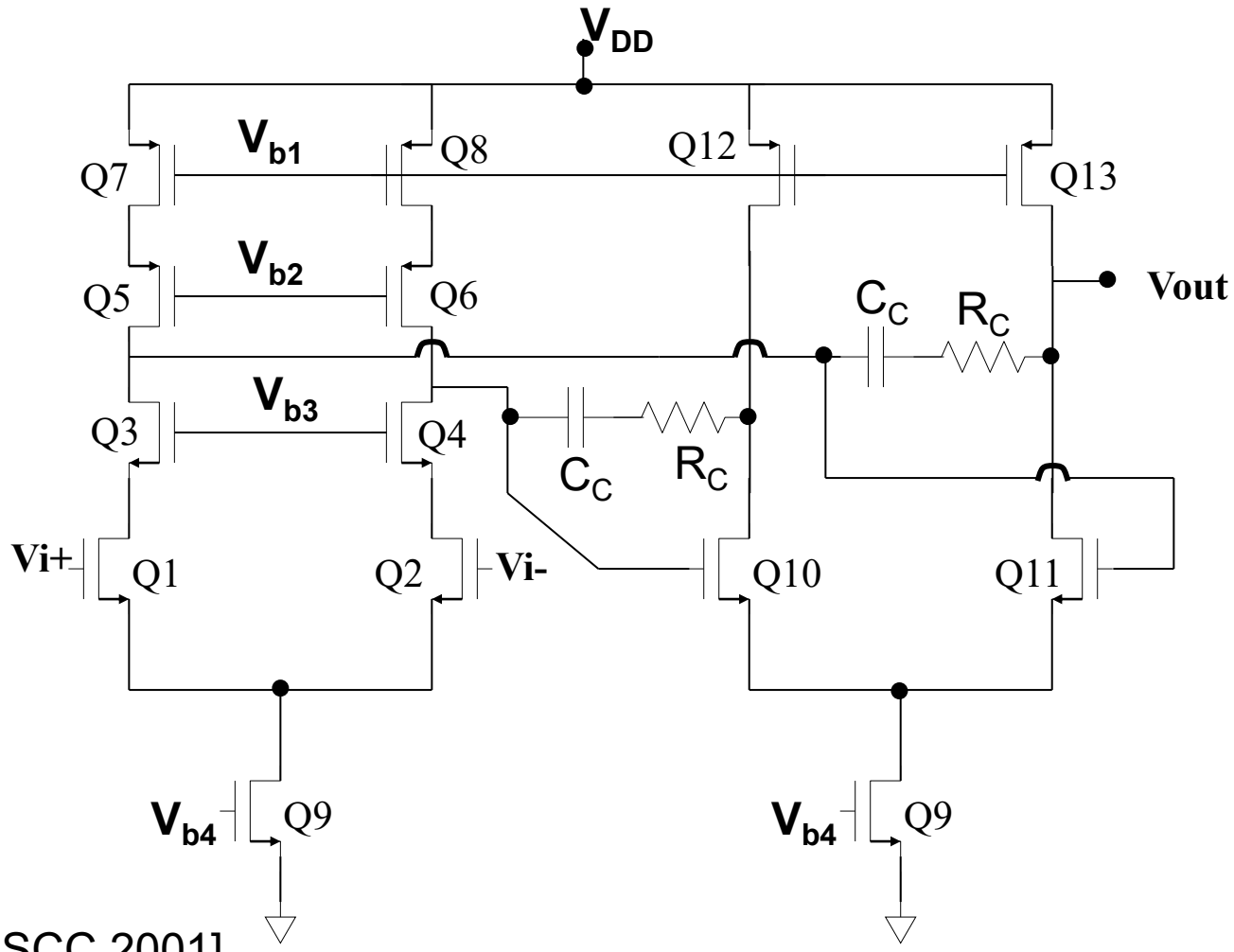
$$A(s) = \frac{(1/2)g_{ml}}{sC_L + [g_{o2} + g_{o4} + g_{o6} + g_{m6} - g_{m4}]}$$

-gm Compensated Single-Stage



CMFB Not Shown

Two-Stage Cascode/Cascade

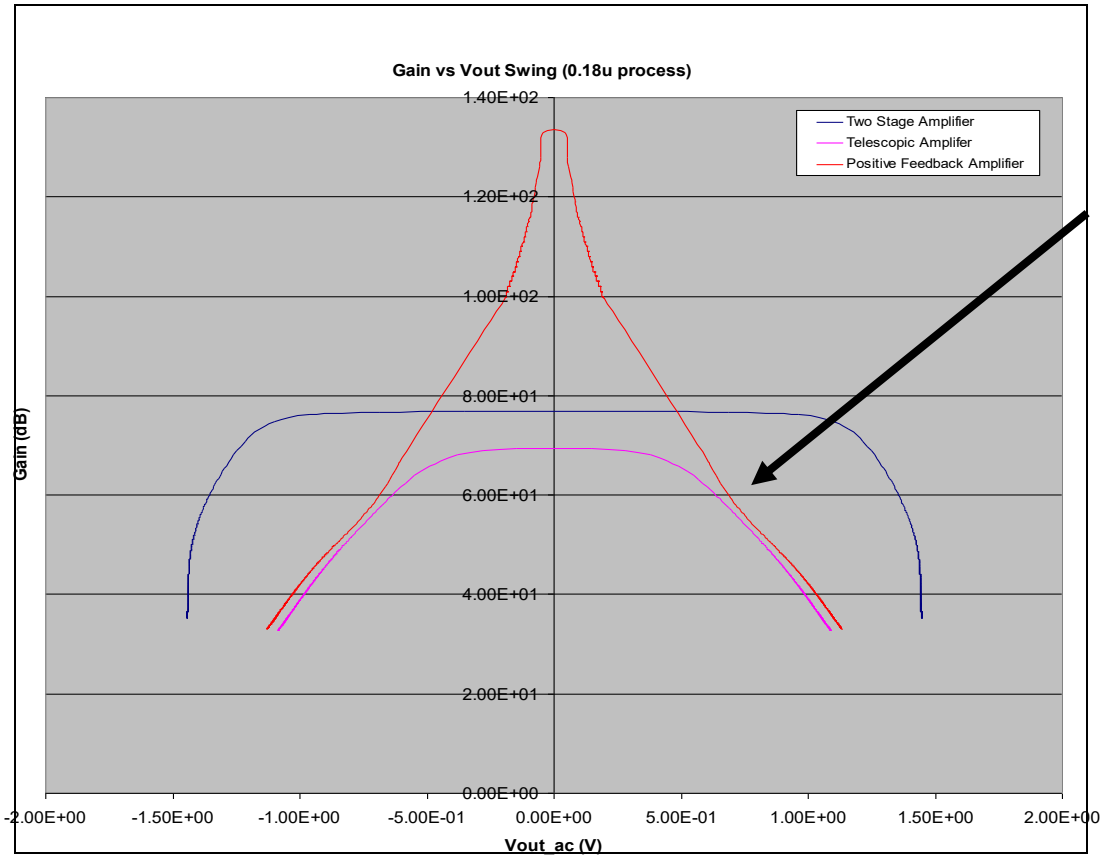


[Park – ISSCC 2001]

CMFB Not Shown

Amplifier Nonlinearity Becoming Increasingly Significant as V_{DD} Reduced

Comparison of amplifiers at same power level and same V_{EB}



Drop in gain seriously degrades linearity and spectral performance

- Nonlinearity strongly architecture dependent
- Trade-Offs between Gain and Signal Swing

How Much Gain?

Depends upon how much of the overall error budget is allocated to the effect noninfinite gain has on required performance parameters

If require n ENOB, can ½ LSB be allocated to effects of op amp gain error?

e.g. If INL specification of a 12-bit ADC is ½ LSB, can ½ LSB be allocated to the noninfinite gain error?

Sources that may contribute to INL errors in pipelined ADC:

Finite Op Amp Gain
Capacitor Missmatch
Incomplete amplifier settling
Amplifier nonlinearity
Input S/H error
Parasitic capacitance nonlinearity
Offset voltage (in ADC, DAC, summer)
DAC errors
ADC nonlinaritry

Error Budgeting

Sources that may contribute to INL errors in pipelined ADC:

Finite Op Amp Gain
Capacitor Missmatch
Incomplete amplifier settling
Amplifier nonlinearity
Input S/H error
Parasitic capacitance nonlinearity
Offset voltage (in ADC, DAC, summer)
DAC errors
ADC nonlinaritry

If entire error budget (e.g. ½ LSB) is allocated to the Finite Op Amp Gain, what error budget must be allocated to all remaining contributors?

What will happen if each error source is allocated an error budget of (e.g. ½ LSB)?

How should the error sources contribution to overall error budget be allocated?

$$\sum_{i=1}^{m} e_i = \frac{1}{2} LSB$$ (maybe a little bit overly conservative)

What type of error budget is used by industry?

Is ENOB equal to the specified number of bits of resolution?

Is it easy to add one additional ENOB of resolution to a given design ?

Why is the ENOB often less than the specified number of bits?

Will consider one example only, others may have ENOB closer or farther from specified resolution

INL-based ENOB

$$ENOB = n_R - 1 - \log_2(\upsilon)$$

Consider an ADC with specified resolution of n_R and INL of v LSB

υ	ENOB
½	n_R
1	n_R-1
2	n_R-2
4	n_R-3
8	n_R-4
16	n_R-5

Though based upon the continuous-INL definition, often used to define ENOB from INL v

ANALOG DEVICES

16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet

$120 in 1000's

AD9467

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- SFDR at 170 MHz at 250 MSPS
  - 92 dBFS at −1 dBFS
  - 100 dBFS at −2 dBFS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - DNL = ±0.5 LSB typical
  - INL = ±3.5 LSB typical
- 2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

$\log_2(3.5)=1.85$

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

FUNCTIONAL BLOCK DIAGRAM

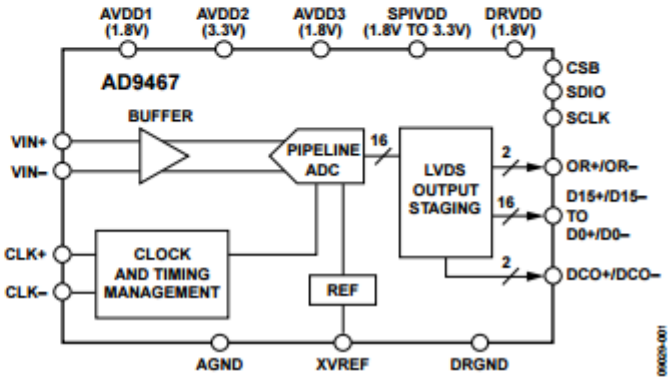


Figure 1.

ENOB $= n_R\text{-}1\text{-}\log_2(\upsilon) = 16 - 1 - 1.85 \cong 13.15$

Is this close to 16-bit performance?

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

Can we depend on this “13-bit” INL performance?

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

$\log_2(12)=3.58$

$$\text{ENOB} = n_R\text{-}1\text{-}\log_2(\upsilon) = 16 - 1 - 3.58 \cong 11.42$$

From INL viewpoint, performance of marketed parts could be about 4.5 bits less than physical resolution but does have other attractive properties

AC SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 5 MHz	25°C		74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C		74.5/76.1		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	73.7	74.3/75.8		dBFS
	Full	71.5			dBFS
f_{IN} = 210 MHz	25°C		74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 5 MHz	25°C		74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	72.4	74.2/75.8		dBFS
	Full	71.0			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 5 MHz	25°C		12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.3		Bits
f_{IN} = 140 MHz	25°C		12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3		Bits
	Full	11.5			Bits
f_{IN} = 210 MHz	25°C		12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		95/93		dBFS
f_{IN} = 140 MHz	25°C		94/95		dBFS
f_{IN} = 170 MHz	25°C	82	93/92		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		93/92		dBFS
f_{IN} = 300 MHz	25°C		93/90		dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 97 MHz at −2 dB Full Scale	25°C		97/97		dBFS
f_{IN} = 140 MHz at−2 dB Full Scale	25°C		100/95		dBFS
f_{IN} = 170 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 210 MHz at −2 dB Full Scale	25°C		93/93		dBFS
f_{IN} = 300 MHz at −2 dB Full Scale	25°C		90/90		dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		97/93		dBFS
f_{IN} = 140 MHz	25°C		97/95		dBFS
f_{IN} = 170 MHz	25°C	88	97/93		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		97/95		dBFS
f_{IN} = 300 MHz	25°C		97/95		dBFS

- Can be defined different ways
- Only given as typical
- Only specified at 25C

How Much Gain?

Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage

Often see authors use $A_{dB} \cong 6n_{ST} + 12$

- Gives no information about drop in gain at boundary of input/output window
- Not dependent upon architecture ?
- Maybe uses too much error budget on gain
- Errors accumulate since gain errors will exist on each stage
- No indication how A_{dB} relates to INL or DNL
- Gain requirements are large on the input buffer (n_{ST}=n) but will be significantly relaxed on latter stages in the pipeline when n_{ST} decreases

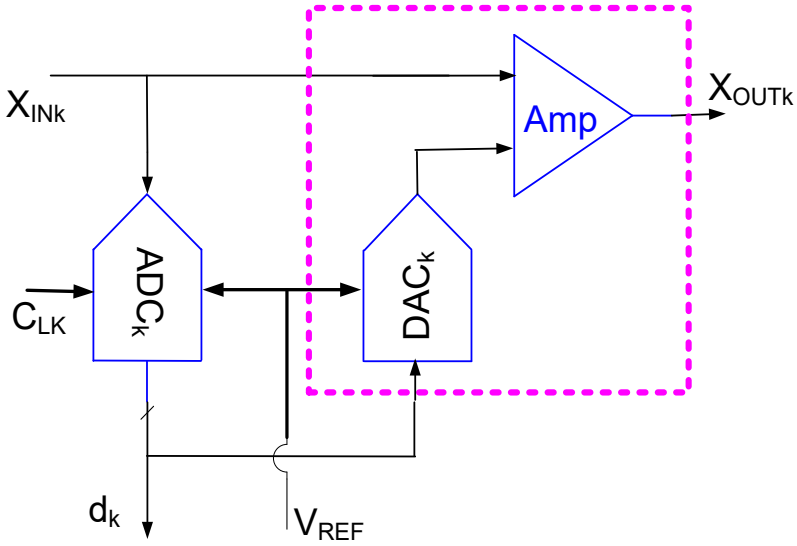
Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors

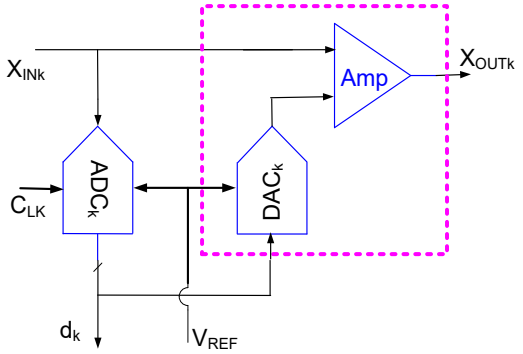
Performance Limitations of Pipelined ADCs

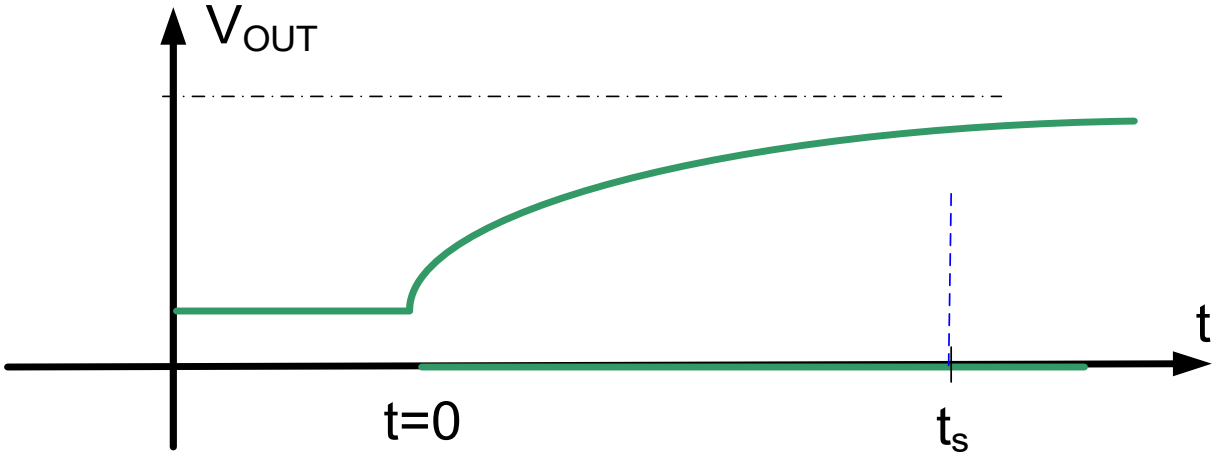
(consider amplifier, ADC and DAC issues)

- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
  - Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Inadequate open loop gain
    - Component mismatch
  - Power Dissipation
  - kT/C switching noise



Amplifier Settling Time

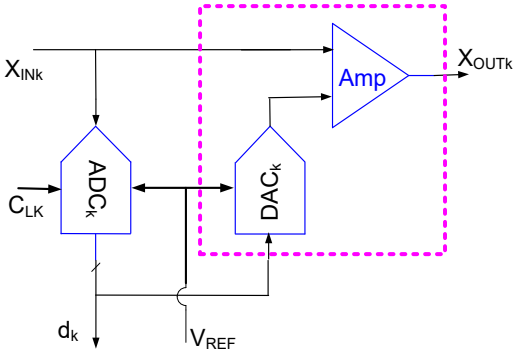




- Can show that no distortion is introduced in pipelined ADC if the amplifier settling is linear (i.e. don't worry about incomplete settling)
- But invariably slew rate and op amp nonlinearities will cause settling to be nonlinear
- Since can't guarantee linear settling, must design for complete settling

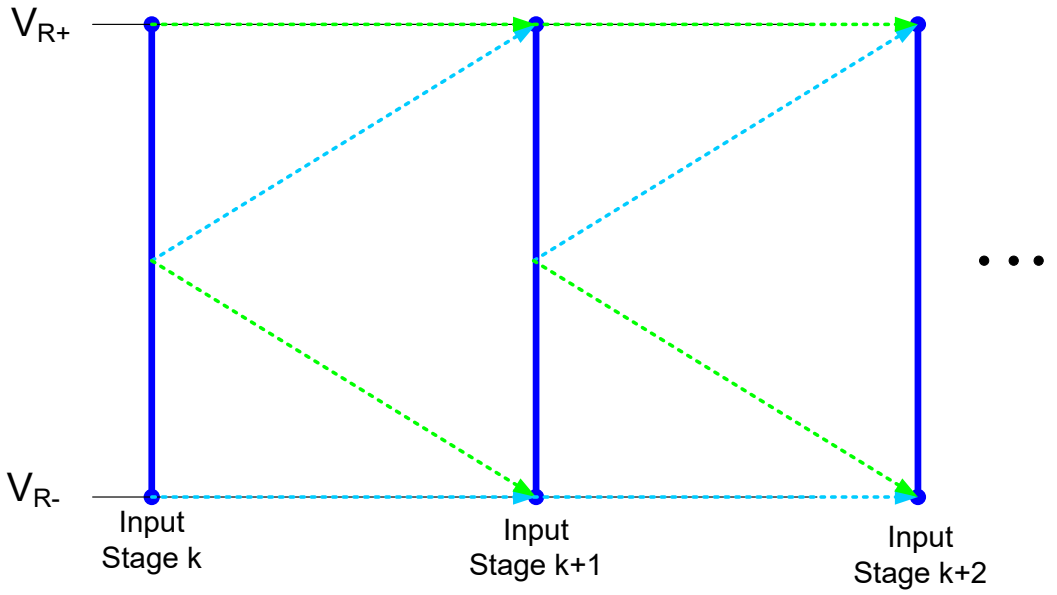
Amplifier Settling Time

Worst Case Settling



- Neglect over-range protection (could be up against over-range limit)
- Occurs when input causes <u>output</u> to swing from 0 to V_{REF}

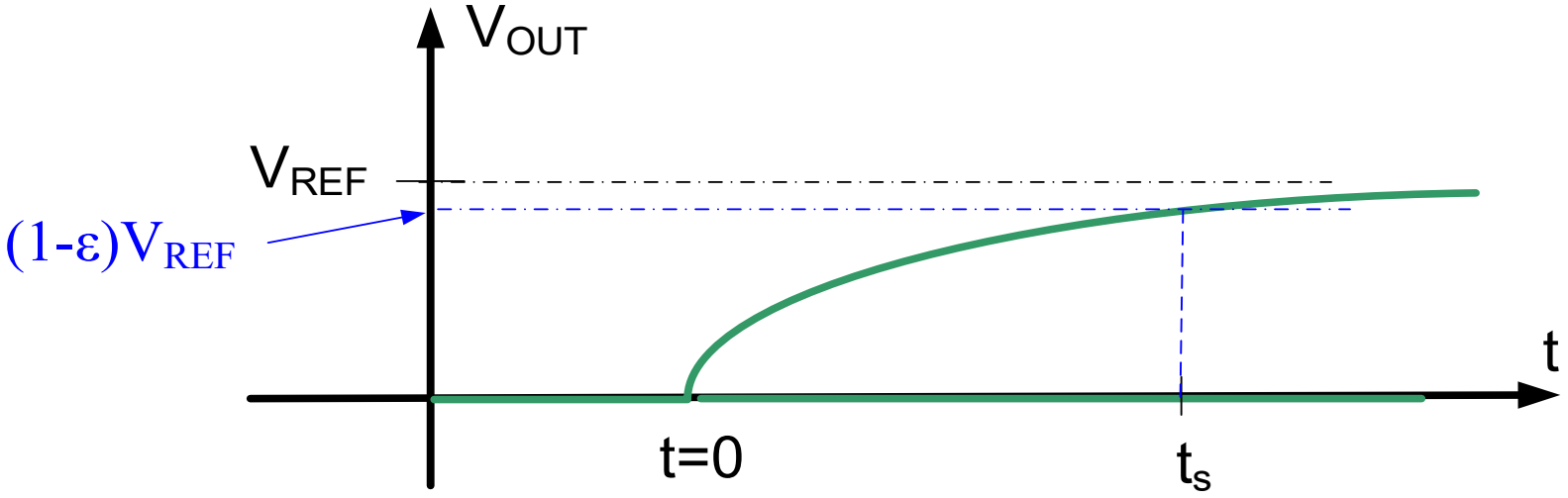
$$V_{REF} = V_{R+} - V_{R-}$$



Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step on output in each stage

Note: This may not be quite good enough since allocating total error budget to settling of each stage

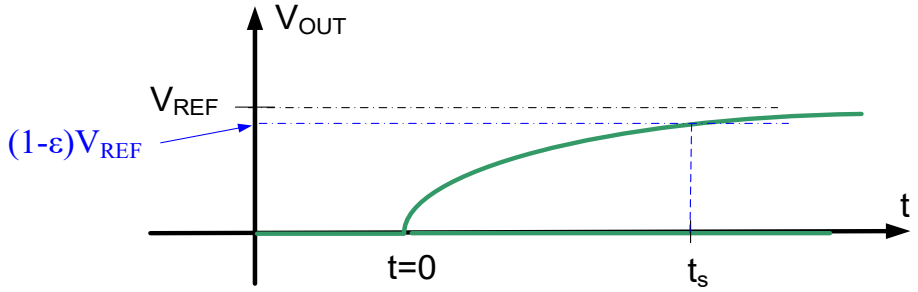


Compensated Operational Amplifier can be approximately modeled by

$$A_{OL}(s) \cong \frac{A_0 p_F}{s+p_F} = \frac{GB}{s+p_F}$$

Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step in each stage



$$A_{OL}(s) \cong \frac{A_0 p_{OL}}{s+p_{OL}} = \frac{GB}{s+p_{OL}} \qquad A_{FB}(s) = \frac{A_0 p_{OL}}{s+p_{OL}+\beta A_0 p_{OL}} \cong \frac{GB}{s+\beta GB}$$

Step response (if slewing is neglected and dc gain large)

$$r(t) = F + (I-F)e^{-\beta GBt_s}$$

$$V_{REF}(1-\varepsilon) = V_{REF}(1-e^{-\beta GBt_s})$$

$$1-\varepsilon = 1-e^{-\beta GBt_s}$$

$$\varepsilon = e^{-\beta GBt_s}$$

$$t_s = -\frac{\ln(\varepsilon)}{\beta GB}$$

or, in terms of the time constant τ of closed loop amplifier

$$t_s = -\tau \ln(\varepsilon)$$

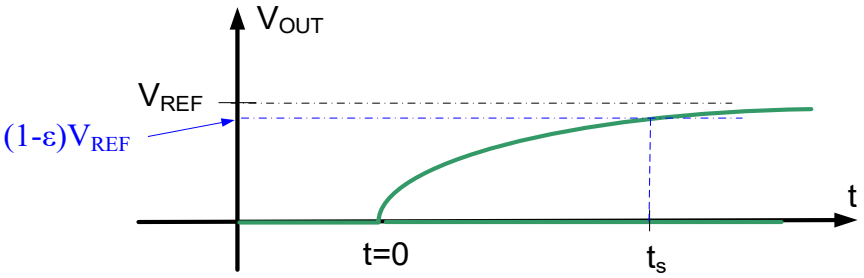
Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step in each stage

Define n_{ST} to be the number of bits of resolution at the residue output of a stage

Step response (if slewing is neglected)

$$\varepsilon = \frac{1}{2^{n_{ST}+1}} \qquad \ln(\varepsilon) = -.693(n_{ST}+1)$$



$$t_s \cong 0.7(n_{ST}+1)\tau$$

- linear increase in settling requirements with n_{ST}
- n_{ST} determined by accuracy requirements at residue output of a stage

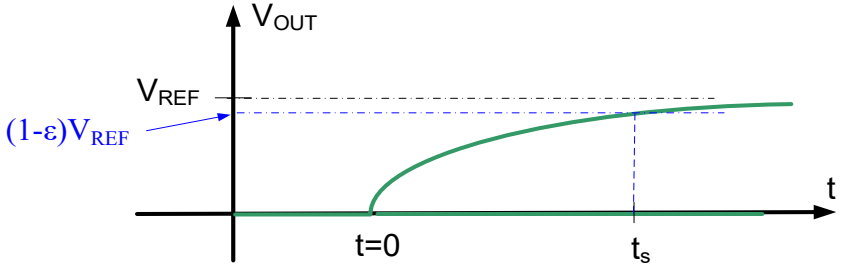
Still need design requirements for GB of Op Amp

$$t_s \cong \frac{0.7(n_{ST}+1)}{\beta GB}$$

Settling Time

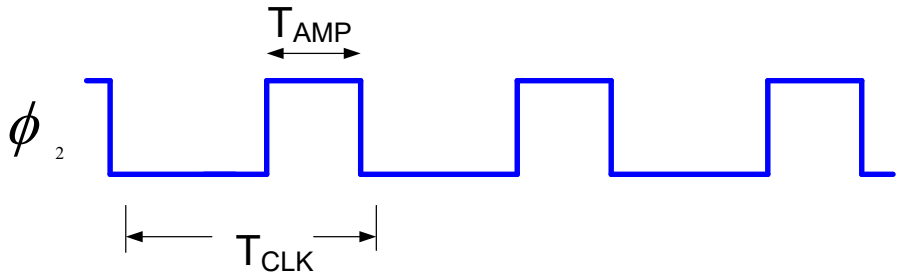
Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step in each stage

Step response (if slewing is neglected)



Design requirements for GB of Op Amp

$$t_s \cong \frac{0.7(n_{ST}+1)}{\beta GB}$$



$$t_s = t_{AMP} \cong \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

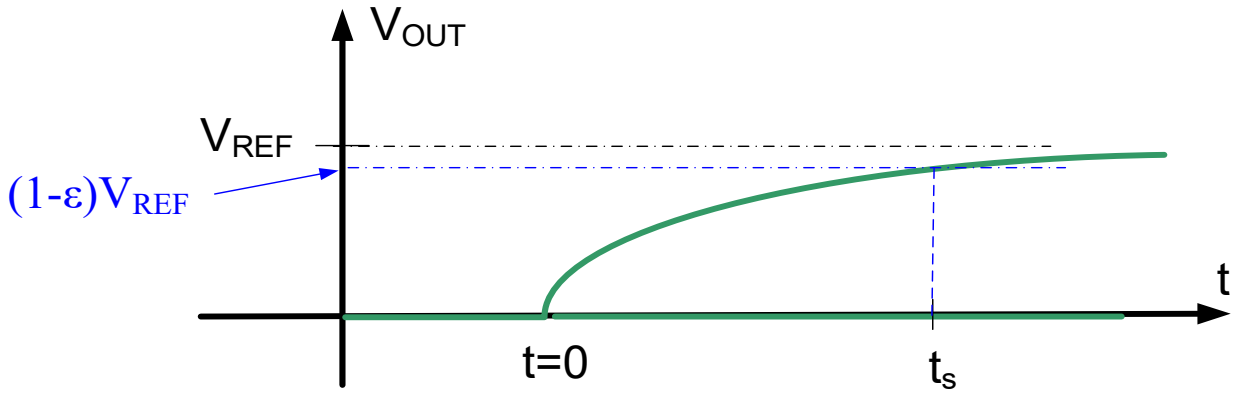
$$GB_{RPS} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK}$$

$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

Note: GB requirements drop from stage to stage

Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step in each stage



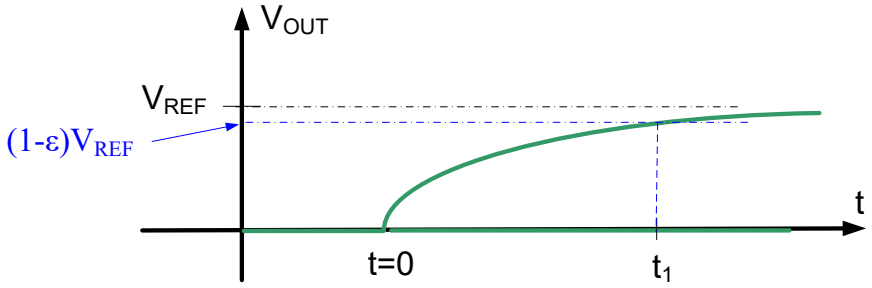
Compensated Operational Amplifier can be approximately modeled by

$$A(s) \cong \frac{A_0 p_F}{s+p_F} = \frac{GB}{s+p_F}$$

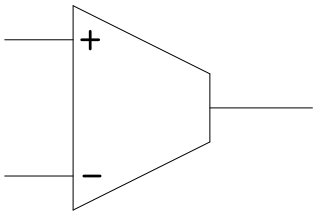
What about high-impedance op amp?

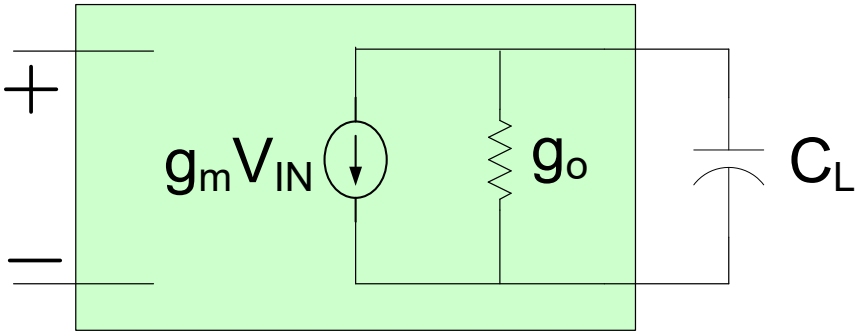
Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step at each stage



What about high-impedance op amp driving capacitive load (including β network)?

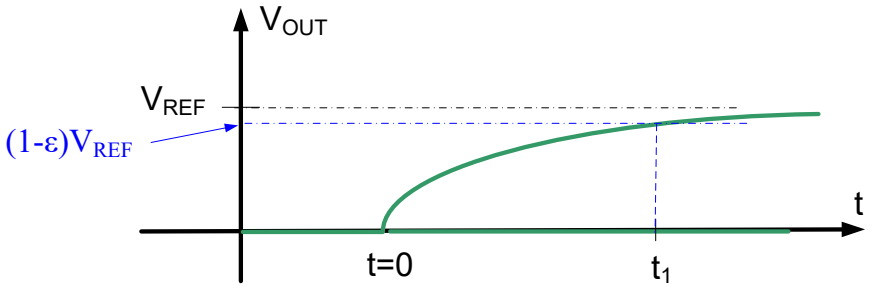




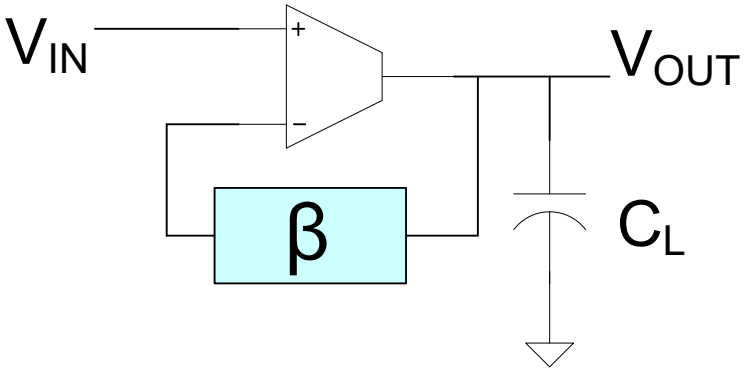
$$A_{OL} = -\frac{g_m}{g_o} \qquad BW = \frac{g_o}{C_L} \qquad GB = \frac{g_m}{C_L}$$

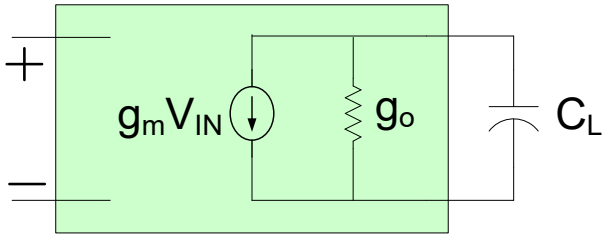
Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step



What about high-impedance op amp?





$$A_{OL} = -\frac{g_m}{g_o} \qquad BW = \frac{g_o}{C_L} \qquad GB = \frac{g_m}{C_L}$$

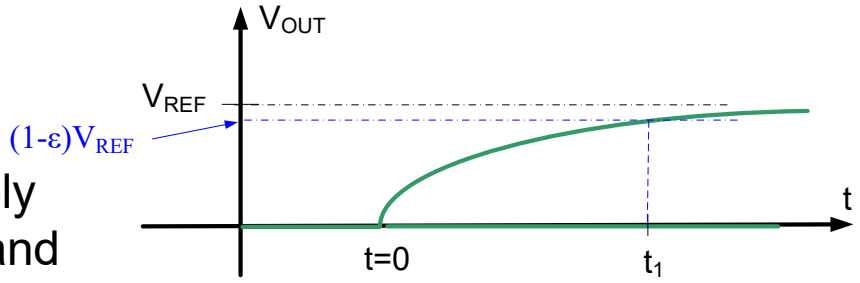
$$A_{FB} = \frac{g_m}{sC_L + g_o + \beta g_m} \cong \frac{g_m}{sC_L + \beta g_m} = \frac{GB}{s + \beta GB}$$

Note this is identical in form to that from the internally compensated op amp

Settling Time

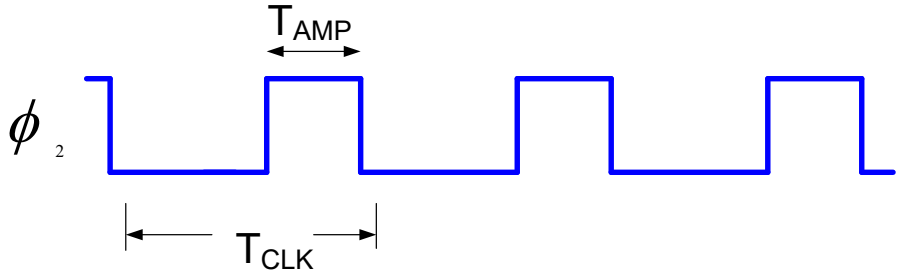
Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step

Step response (if slewing is neglected)



Design requirements for GB of Op Amp apply to both compensated two-stage structures and high output impedance single-stage structures

$$t_s \cong \frac{0.7(n_{ST}+1)}{\beta GB}$$



$$t_s = t_{AMP} \cong \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

$$GB_{RPS} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK}$$

$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

Notes: May be over-using error budget
Slewing will modestly slow response

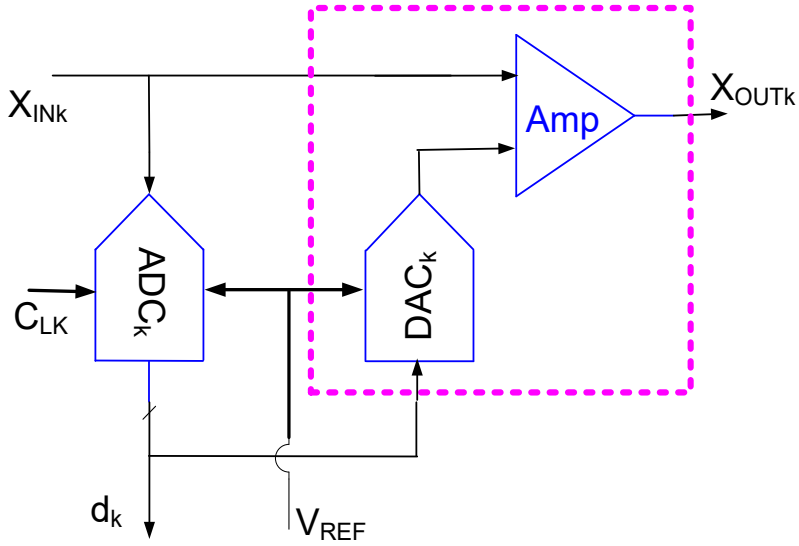
Pipelined Data Converter Design Guidelines

	Issue		Strategy
1.	ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1.	Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2.	Op Amp Gain causes finite gain errors and introduces noninearity	2.	a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3.	Op amp settling must can cause errors	3.	Select GB to meet settling requirements (degrade modestly to account for slewing)

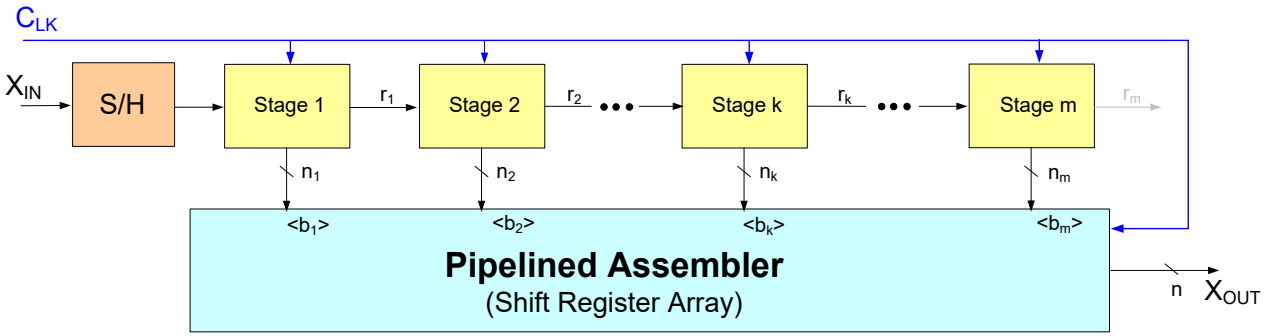
Performance Limitations of Pipelined ADCs

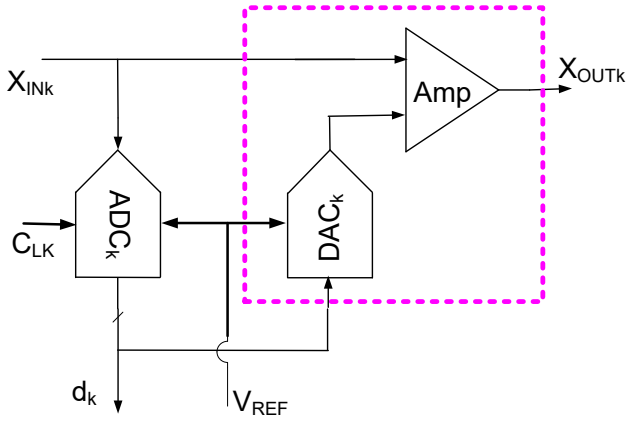
(consider amplifier, ADC and DAC issues)

- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
  - Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Inadequate open loop gain
    - Component mismatch
  - Power Dissipation
  - kT/C switching noise



Power Dissipation

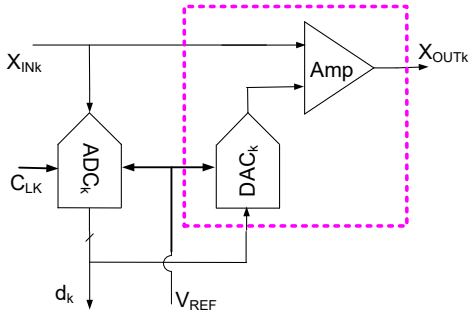




Dominant source of power dissipation is in the op amps in S/H and individual stages

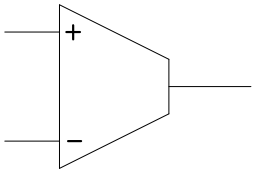
Power Dissipation

- Power dissipation strongly dependent upon op amp architecture and design
- Power budgets critical and even a net 5% savings in power is significant!



Consider a single stage in the pipeline

Consider single stage open-loop op amp structures (e.g. telescopic cascode)

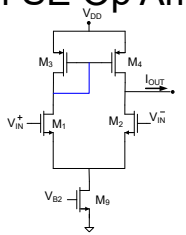


$$A_{OL} = -\frac{g_{mT}}{g_{oT}}$$

$$P_{OP\ AMP} \cong 2I_{DQ}\left(V_{DD} - V_{SS}\right)$$

Power increases linearly with I_{DQ}

Ref SE Op Amp



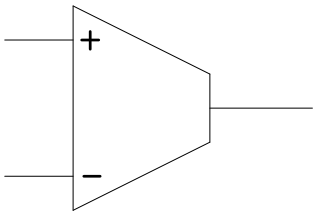
For MOS implementation with basic reference SE op amp

$$A_{OL} = -\frac{2I_{DQ}}{V_{EB}}\frac{1}{2\lambda I_{DQ}} = -\frac{1}{\lambda V_{EB}}$$

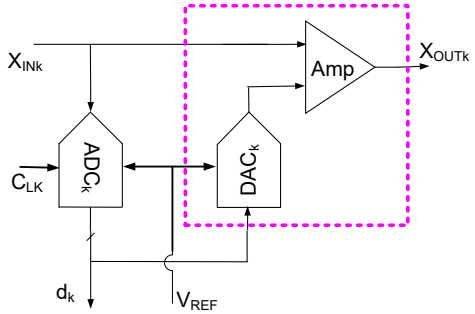
No power implications on dc gain of op amp

- Pick V_{EB} small to increase gain
- Keep lengths larger than minimum to make λ small

Power Dissipation



$$GB = \frac{g_{mT}}{C_L}$$



C_L is the parallel combination of any interconnect capacitance, the capacitance of the β network and the sampling capacitance of the following stage

For MOS implementation (with ref SE op amp or telescopic cascode op amp)

$$GB = \frac{2I_{DQ}}{V_{EB}C_L} = \left(\frac{1}{(V_{DD}-V_{SS})}\frac{P}{C_L}\right)\frac{1}{V_{EB}}$$

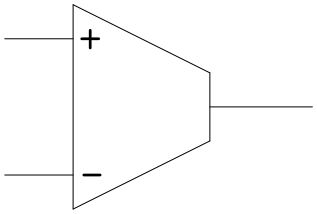
For convenience, define

$$V_{SUP} = V_{DD} - V_{SS}$$

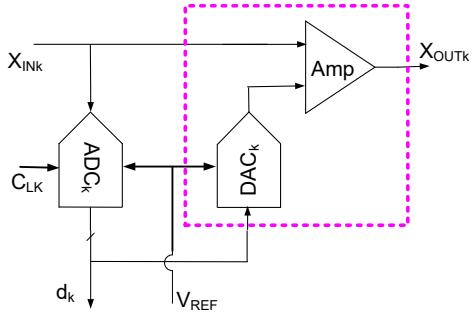
$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$

- P increases linearly with GB
- Keep V_{EB} small, C_L as small as possible, GB as small as possible
- At high speeds, diffusion parasitics will cause P to increase more rapidly than GB
- Total amplifier power is sum of power in each stage

Power Dissipation

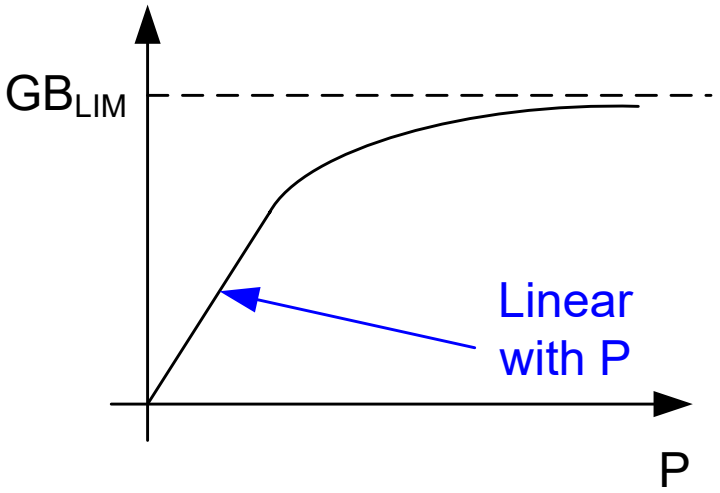


$$GB = \frac{g_m}{C_L}$$



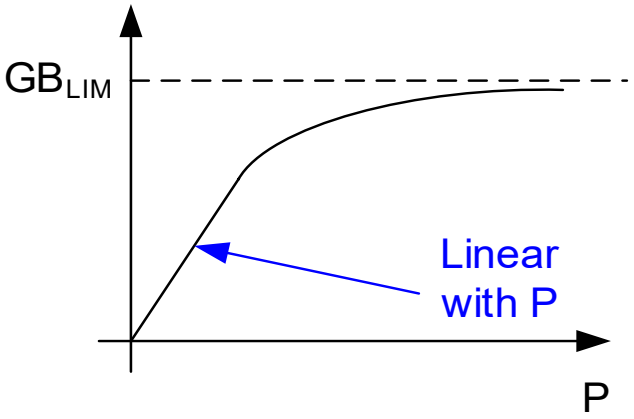
For single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$

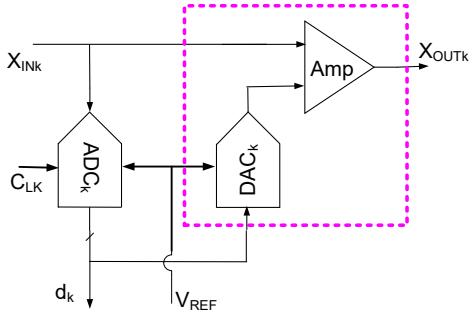


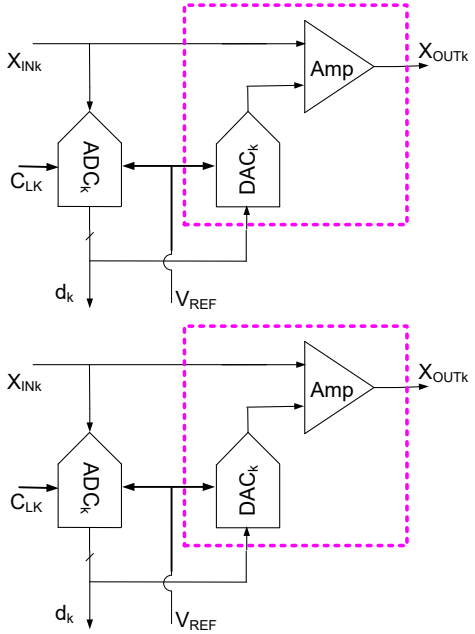
At high speeds, diffusion parasitics will cause P to increase more rapidly than GB

Power Dissipation



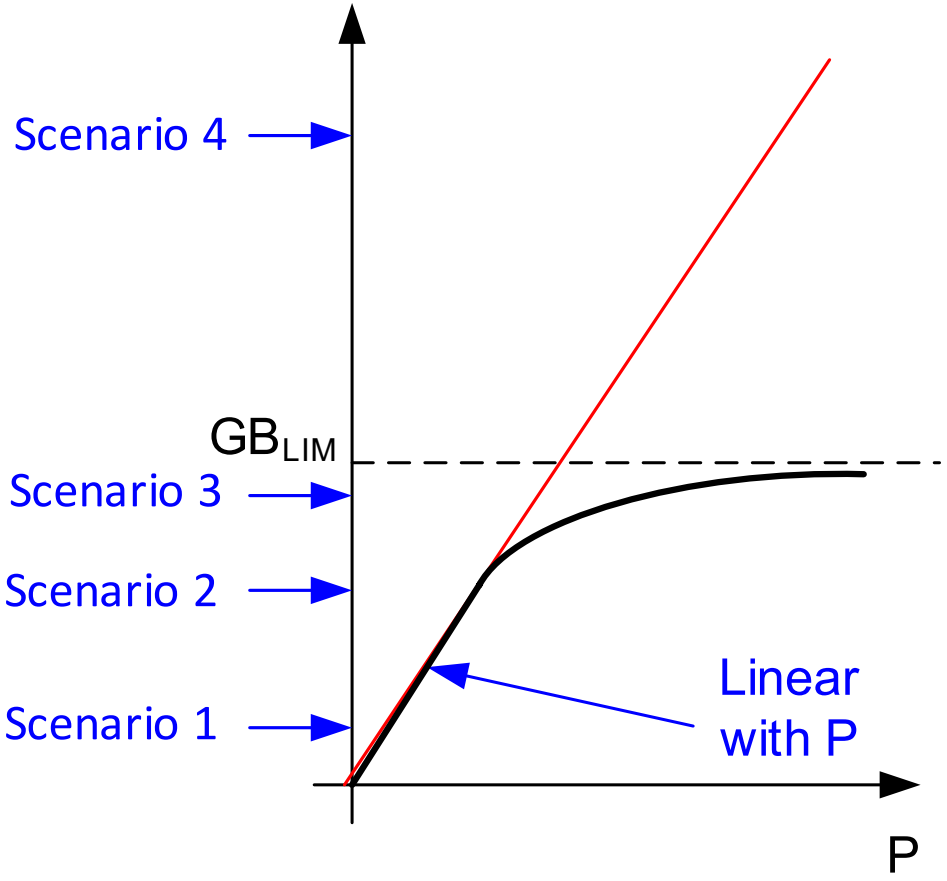
$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$





Interleaving can dramatically reduce power requirements (e.g. two interleaved stages reduce GB requirements a factor of 2 on each stage thereby maintaining power requirements on linear slope region) for high speed data converters but introduces some calibration challenge**s**

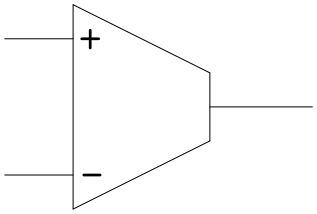
Power Dissipation



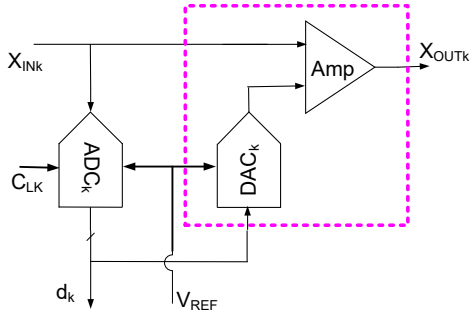
GB_{LIM} strongly technology dependent

What do we do if system requirements are in the respective scenarios?

Power Dissipation



$$GB = \frac{g_m}{C_L}$$



For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

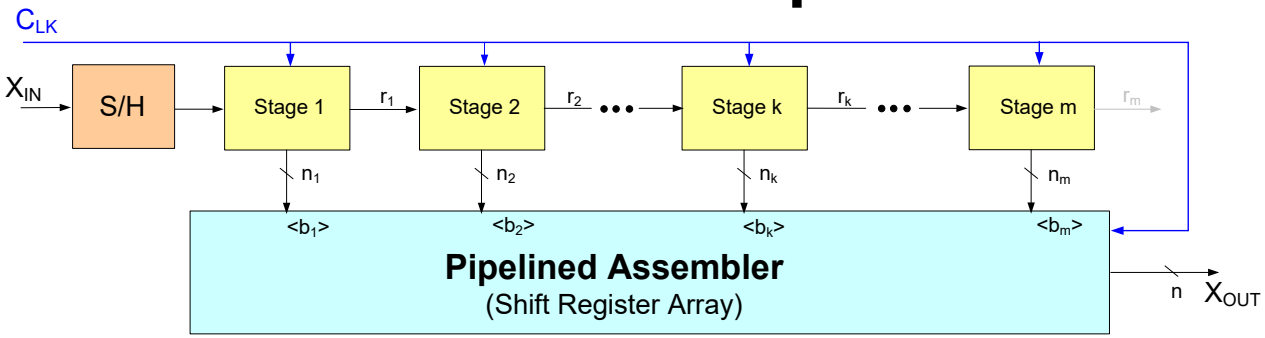
$$P = [V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

Architecture Dependent

Select architectures that minimize architecture-dependent term

Power Dissipation



For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

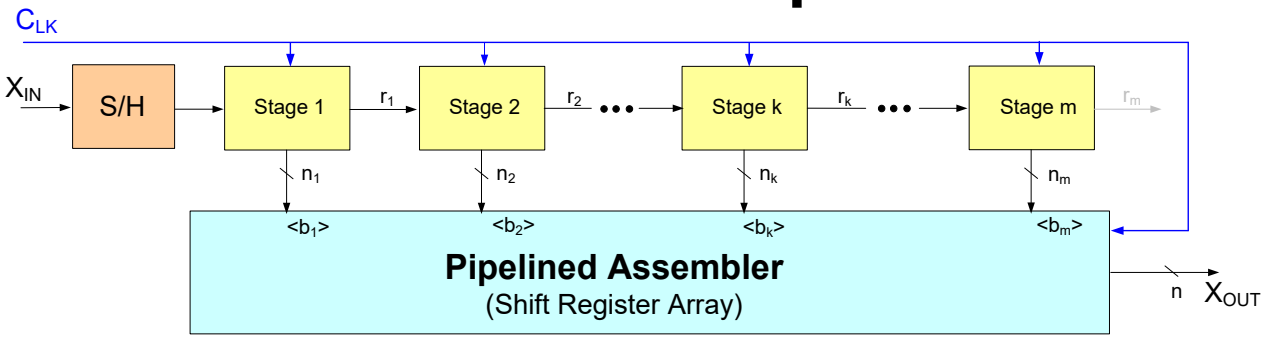
$$P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

- n_{ST}=n for S/H thus S/H is a major power consumer
- Use energy efficient op amp architecture
- Power increases linearly with GB (even faster at high frequencies)
- Interleaving can reduce power dissipation at high frequencies(and extend effective clock speed)
- Power increases linearly with clock speed (or worse at high frequencies)
- Power can be scaled down in latter stages since n_{ST} will decrease
- Amplifiers can be shared between stages or switched off when not used (factor of 2!)
- Using more than one bit/stage will reduce power since no of op amps will decrease (offsets decrease in β)
- Elimination of S/H will have dramatic effect on power reduction

Power Dissipation



For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

$$P = [V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

Which op amp architectures are most energy efficient?

- Depends upon β
- For smaller β, two-stage are more energy efficient for larger β single-stage are better
- Must optimize power in any given architecture
- Folding reduces efficiency (typically by 30% to 50%)

V. Katyal, Y. Lin, and R. L. Geiger, "Power Dependence of Feedback Amplifiers on Op Amp Architecture," *IEEE Int. Symposium on Circuits and Systems*, Kobe, Japan, May 2005, pp. 1618-1621.

Stay Safe and Stay Healthy !

End of Lecture 24

End of Lecture 21
From Spring 2019